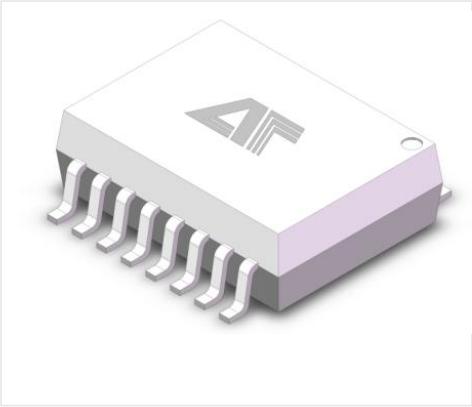
AOTE SEMICONDUCTOR



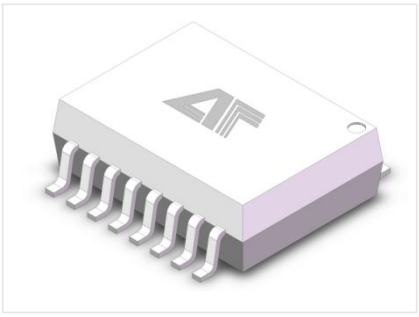
智能栅极驱动光耦
Intelligent gate driven optocoupler

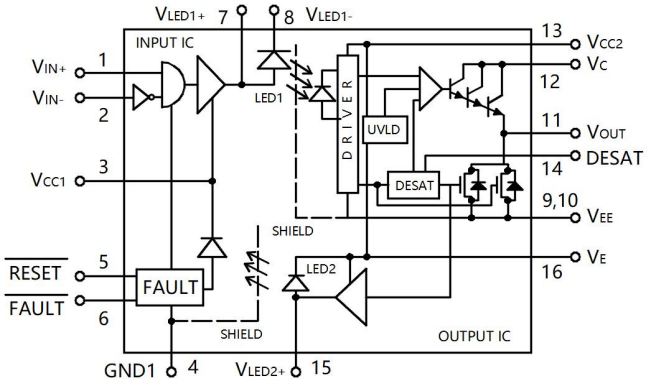
AT316J

Product Data Sheet

AOTE DCC
RELEASE

SOP16





◆ 封装逻辑原理图 Encapsulation logic schematic

AT316J 光耦采用高效光电转换技术，结合先进封装工艺，提供输入输出间的可靠隔离，支持SOP16封装形式，适配多样化场景需求。The AT316J optocoupler adopts high-efficiency photoelectric conversion technology and advanced packaging processes, providing reliable input-output isolation. It supports package types SOP16 to meet diverse application requirements.

◆ 产品特征Product features

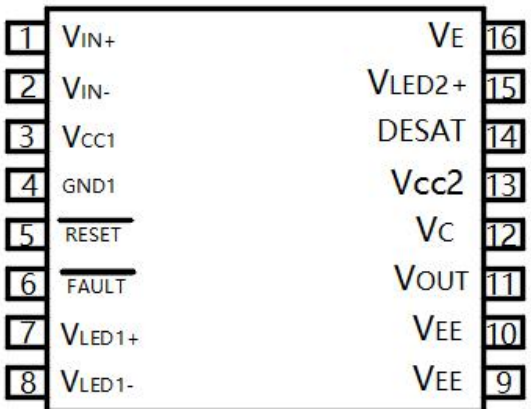
- 输入-输出隔离电压Vios=5000Vrms ； Input output isolation voltage：Vios=5000Vrms
- 15 kV/μs最小共模抑制;15 kV/μs minimum Common Mode Rejection
- 15V 至 30V 宽工作电压范围；15V ~ 30V Wide operating VCC Range
- 峰值输出电流2.5A;peak output current2.5A
- 输出级可驱动150A和1200V 的 IGBTs；The output stage can drive IGBTs with 150A and 1200V；
- 爬电距离>7.0mm ; Creepage distance > 7.0mm；
- 输入-输出绝缘距离 >0.4mm ； Input-Output insulation Thickness > 0.4mm
- 防潮等级 class1； MSL class1
- 产品符合 ROHS、REACH 及 HF 等环保法规要求；The products comply with ROHS, REACH and HF；

◆ 应用领域 Applications

- **工业自动化设备:** industrial automation equipment;用于逆变器、交流伺服器,提升系统稳定性和能效；Used for inverters, communication servers, improving system stability and energy efficiency；
- **汽车电子系统：** Automotive Electronic Systems；用于电动汽车的电机驱动，电子刹车系统，增强安全性和开关效率；Motor drive for electric vehicles, Electronic brake system enhances safety and switch efficiency
- **新能源发电领域:** In the field of new energy generation;在光伏、风力发电等,优化电能转换与传输过程Optimize the process of energy conversion and transmission in photovoltaic, wind power generation, etc;
- **电力输送系统：** Power transmission system；支持高压直流输电和柔性交流输电系统，保障输电线路的稳定运行 Support high-voltage direct current transmission and flexible alternating current transmission systems, Ensure the stable operation of transmission lines




◆ 引脚功能说明：pin Function Description



脚 pin	符号 symbol	描述 Description	
1	VIN+	非反相门驱动电压输出(VOUT)控制输入	Noninverting gate drive voltage output (VOUT) control input
2	VIN-	反相门驱动电压输出(VOUT ） 控制输入	Inverting gate drive voltage output (VOUT) control input
3	VCC1	正向输入电源电压。(4.5 V 至 5.5 V)	positive input supply voltage. (4.5 V to 5.5 V)
4	GND1	输入地	Input Ground
5	$\overline{\text{RESET}}$	FAULT 复位输入。逻辑低输入至少 0.1μs ，异步复 位 FAULT 输出高 ，并启用 VIN。需要同步控制RESET 相对于 VIN。RESET 不受 UVLO 影响。在 VOUT 高时断言 RESET 不会影响 VOUT。	FAULT reset input. A logic low input for at least 0.1 μs，asynchronously resets FAULT output high and enables VIN. Synchronous control of RESET relative to VIN is required. RESET is not affected by UVLO. Asserting RESET while VOUT is high does not affect VOUT.
6	$\overline{\text{FAULT}}$	错误输出。当 DESAT 脚超出内部参考电压 7V 时 ，FAULT 脚将输出一个集电极开路的信号 ，在 5us 内 FAULT 脚将从高阻状态转变成一个逻辑低 电平。FAULT 输出一直很低 ，直到 RESET 值降 低。AT316J 的 FAULT 输出是一个集电极开路 ，在同一电路的单个的 FAULT 脚以 “或” 逻辑连接成 一条母线到单片机。	FAULT output. FAULT changes from a high impedance state to a logic low output within 5μs of the voltage on the DESAT pin exceeding an internal reference voltage of 7V. FAULT output remains low until RESET is brought low. FAULT output is an open collector which allows the FAULT outputs from all AT316J in a circuit to be connected together in a “wired OR” forming a single fault bus for interfacing directly to the micro-controller.
7	VLED1+	LED1 阳极。为了保证数据手册的性能 ，此引脚必 须保持不连接。(仅用于光耦测试)	LED1 anode. This pin must be left unconnected for guaranteed data sheet performance. (For optical coupling testing only.)
8	VLED1-	LED1 阴极。该引脚必须与接地相连接。	LED1 cathode. This pin must be connected to ground.
9	VEE	输出电源电压	Output supply voltage
10	VEE	输出电源电压	Output supply voltage
11	VOUT	栅极驱动电压输出	Gate drive voltage output
12	VC	输出电源电压。	positive output supply voltage
13	VCC2	正输出电源电压	positive output supply voltage
14	DESAT	去饱和电压输入引脚。当 DESAT 脚电压在 IGBT 导通时超过内部参考电压 7V ，故障输出端将在 5us 内从高阻状态转变成一个逻辑低电平。	Desaturation voltage input. when the voltage on DESAT exceeds an internal reference voltage of 7V while the IGBT is on，FAULT output is changed from a high impedance state to a logic low state within 5 μs.
15	VLED2+	LED2 阳极。为了保证数据手册的性能 ，此引脚必 须保持不连接。(仅用于光耦测试)	LED2 anode. This pin must be left unconnected for guaranteed data sheet performance. (For optical coupling testing only.)
16	VE	公共(IGBT 发射极)输出电源电压。	Common (IGBT emitter) output supply voltage

◆ 极限参数 Absolute Maximum Ratings (Ta =25℃)

参数 Parameter		符号 Symbol	最小值 Min.	最大值 Max.	单位 Unit
发射端 Input	正输入电源电压 positive Input supply voltage	Vcc1	-0.5	5.5	V
	输入引脚电压 Input pin voltages	VIN+, VIN- and VRESET	-0.5	5.5	V
	输入 IC 功率耗散 Input IC Power Dissipation	PI	-	150	mW
输出端 Output	峰值输出电流 peak output current	Io(peak)	-	2.5	A
	故障输出电流 Fault output current	IFAULT	-	10	mA
	总输出电源电压 Total output supply voltage	Vcc2 - VEE	-0.5	30	V
	反向输出电源电压 Negative output supply voltage	VE - VEE	-0.5	15	V
	正向输出电源电压 positive output supply voltage	Vcc2 - VE	-0.5	35 - (VE - VEE)	V
	栅极驱动输出电压 Gate Drive output voltage	VO(peak)	-0.5	Vcc2	V
	集电极电压 collector voltage	VC	VEE + 5 v	Vcc2	V
	DESAT 电压 DESAT voltage	VDESAT	VE	VE + 10	V
	输出IC 结温度 output IC Junction Temperature	TJ	-40	125	℃
	输出 IC 功率耗散 output IC Power Dissipation	Po	-	600	mW
隔离电压 Isolation Voltage		Viso	5000		Vrms
工作温度 Operating Temperature		Topr	-55 ~+110		℃
存储温度 Storage Temperature		Tstg	-55 ~+125		℃
焊接温度 Soldering Temperature		Tsol	260		℃

◆ 推荐操作条件 Recommended Operating Conditions

参数 Parameter	符号 Symbol	最小值 Min	最大值 Max.	单位 Unit
工作温度 operating Temperature	TA	-40	+110	℃
输入电源电压 Input supply Voltage	VCC1	4.5	5.5	V
总输出电源电压 Total output supply Voltage	VCC2 - VEE	15	30	
负输出电源电压 Negative output supply Voltage	VE - VEE	-0.5	15	
正输出电源电压 Positive output supply Voltage	VCC2 - VE	-0.5	30 - (VE - VEE)	
集电极电压 Collector Voltage	VC	VEE + 6	VCC2	
峰值高电平输出电流 Peak high-level output current	IOPH	-	2.5	A
峰值低电平输出电流 Peak low-level output current	IOPL	-	2.5	A
DEsAT 电压 DEsAT Voltage	VDESAT	VE	VE +10	V
输出 IC 功率散 output IC Power Dissipation	Po	-	600	mw
工作频率 operating frequency	f	-	50	KHz

◆ 产品特性参数Product characteristic parameters (Ta =25℃)

除非另有说明， 典型值测量值在 TA =25℃, VCC2 - VEE = 30 V, VE - VEE = 0 V 测得； 所有的最小/最大规格遵照推 荐工作条件。Unless otherwise noted, all typical values at TA =25℃, VCC2 - VEE = 30 V, VE - VEE = 0 V; All Minimum/Maximum specifications are at Recommended Operating Conditions.

参数 Parameter	符号 Symbol	条件 Condition	最小 Min.	典型 Typ.	最大 Max.	单位 Unit	备注 Note
逻辑低输入电压 Logic Low Input Voltages	VIN+L, VIN-L VRESETL	-	-	-	0.8	V	-
逻辑高输入电压 Logic High Input Voltages	VIN+H, VIN-H VRESETH	-	2.0	-	-		-
逻辑低输入电流 Logic Low Input Current	IIN+L, IIN-L IRESETH	VIN = 0.4 V	-0.5	-0.4	-	mA	-
故障逻辑低输出电流FAULT Logic Low Output Current	IFAULTL	VFAULT = 0.4 V	5.0	12	-		25
故障逻辑高输出电流FAULT Logic High Output Current	IFAULTH	VFAULT = VCC1	-40	-	-	μA	26
高电平输出电流 High Level Output Current	IOH	VOUT = VCC2 - 4V	-0.5	-1.5	-	A	1, 6, 27
		VOUT = VCC2 - 15 V	-2.0	-	-		
低电平输出电流 Low Level Output Current	IOL	VOUT = VEE +1.5 V	1.0	-	-		2, 7, 28
		VOUT = VEE + 4.0 V	2.5	-	-		
故障状态下的低电平输出电流 Low Level Output Current During Fault Condition	IOLF	VOUT - VEE =14 V	90	140	230	mA	3, 29
高电平输出电压 High Level Output Voltage	VOH	OUT = -100 mA	VC-3.5	VC -2.5	-	V	4, 6, 30
低电平输出电压 Low Level Output Voltage	VOL	IOUT = 100 mA	-	0.1	0.5		5, 7, 31
高电平输入电源电流High Level Input Supply Current	ICC1H	VIN+ = VCC1 = 5.5 V VIN- = 0 V	-	16	22	mA	8, 32, 33
低电平输入电源电流 Low Level Input Supply Current	ICCIL	VIN+ = VIN- = 0 V, VCC1 = 5.5 V	-	3	11		
输出电源电流 Output Supply Current	ICC2	VOUT = Open	-	2.5	5		9, 10, 34, 35
低电平集电极电流 Low Level Collector Current	ICL	IOUT = 0	-	0.3	1.0		13, 54
高电平集电极电流 High Level Collector Current	ICH	IOUT = 0	-	0.3	1.3		13, 53

参数 Parameter	符号 Symbol	条件 Condition	最小 Min.	典型 Typ.	最大 Max.	单位 Unit	备注 Note
VE 低电平供电电流 VE Low Level Supply current	IEL	-	-0.7	-0.4	0	mA	12,56
VE 高电平供电电流 VE High Level Supply current	IEH	-	-0.5	-0.14	0	mA	12,35
消隐电容器充电电流 Blanking capacitor charging current	IcHG	VDESAT = 0 - 6 V, VDESAT = 0 - 6 V, TA = 25 - 100℃	-0.13	-0.24	-0.33	mA	11,36
消隐电容器放电电流Blanking capacitor Discharge current	IDScHG	VDESAT = 7 V	10	30	-	mA	37,38
UVLO 國值 UVLO Threshold	VUVLO+	IF =10mA, VOUT > 5 V	11.6	12.3	13.5	V	-
	VUVLO-	IF =10mA, VOUT < 5 V	9.2	11.1	12.4	V	-
UVLO 滞后 UVLO Hysteresis	VUVLO+ - VUVLO-	-	-	1.2	-	V	-
DESAT 國值 DESAT Threshold	VDESAT	Vcc2 - VE > VUVLO-	6.0	6.7	7.5	V	14,39
输入國值电流从低到高Threshold input current Low to high	IF(ON)	Io = 0mA, Vo > 5.0V	-	2.0	5.0	mA	-
输入國值电压从高到低Threshold input voltage High to low	VF(OFF)	Io = 0mA, Vo < 5.0V	0.6	-	-	V	-

◆ 开关特性参数Switch characteristic parameters

除非另有说明， TA = 25°C、VCC2 = 30 V、VEE 接地时的所有典型值； 所有最小/最大规格都是在推荐的工作条件下。
Unless otherwise noted, all typical values at TA = 25°C, VCC2 = 30 V, VEE = Ground; All Minimum/Maximum specifications are at Recommended Operating Conditions.

参数 Parameter	符号 Symbol	条件 Condition	最小 Min.	典型 Typ.	最大 Max.	单位 Unit	备注 Note
V_{IN} 到高水平输出传播延迟时间 V_{IN} to High Level Output propagation Delay Time	T_{PLH}	Rg = 10 Ω, cg = 10 nF, f = 10 kHz, Duty cycle = 50%	0.10	0.30	0.50	μs	15, 16, 17, 18, 19, 20, 40, 49, 50
V_{IN} 到低电平输出 传播延迟时间 V_{IN} to Low Level Output propagation Delay Time	T_{PHL}		0.10	0..32	0.50		
脉冲宽度失真 pulse Width Distortion	PDW		-300	20	300	ns	-
任意两个部分之间的传播延迟差 propagation Delay Difference Between Any Two parts	PDD		-100	-	100		-
10%至 90%的上升时间 10% to 90% Rise Time	Tr		-	50	-		40
90%到 10%的下降时间 90% to 10% Fall Time	Tf		-	50	-		
DESAT 意义到 90%的 VOUT 延迟 DESAT Sense to 90% VOUT Delay	T_{DESAT} (90%)	Rg=10Ω, Cg=10nF	-	0.3	0.5	us	21,51
DESAT 意义到 10%的 VOUT 延迟 DESAT Sense to 10% VOUT Delay	T_{DESAT} (10%)	VCC2-VEE =30V	-	2.0	3.0		22,51,41
DESAT 检测到低电平故障信号延迟 DESAT Sense to Low Level FAULT Signal Delay	T_{DESAT} (FAULT)	-	-	1.8	5		42,51
DESAT翻转到DESAT低电平传播延迟时间 DESAT Sense to DESAT Low Propagation Delay	T_{DESAT} (LOW)	-	0.1	0.25	1.0		51
DESAT翻转到低电平故障信号延迟时间 DESET to High Level FAULT Signal Delay	T_{RESET} (FAULT)	-	3	7	20		23,51
故障信号脉冲宽度 RESET Signal Pulse Width	PW RESET	-	0.1	-	-		-
UVLO到VOUT的高延迟 UVLO to VOUT High Delay	$T_{UVLO(ON)}$	-	-	5.0	-		44
UVLO到VOUT的低延迟 UVLO to VOUT Low Delay	$T_{UVLO(OFF)}$	VCC2=1.0ms ramp	-	5.0	-		
输出高电平共模瞬态抗扰度 Output High Level Common Mode Transient Immunity	|CMH|	TA=25°C, VCM=1500V, VCC2=30V	15	30	-	Kv/us	45,46,47,48
输出低电平共模瞬态抗扰度 Output Low Level Common Mode Transient Immunity	|CML|	TA=25°C, VCM=1500V, VCC2=30V	15	30	-		

◆ 电性特性曲线Electrical characteristic curve(Ta =25℃)

Fig.1 Output High Current vs Ambient Temperature

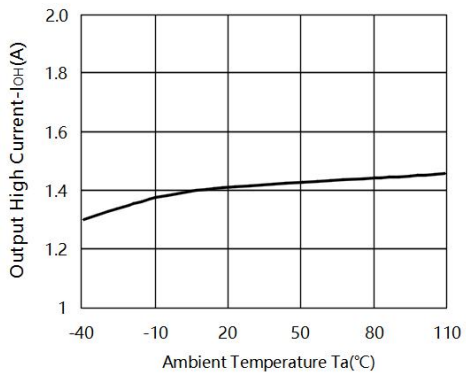


Fig.2 Output Low Current vs Ambient Temperature

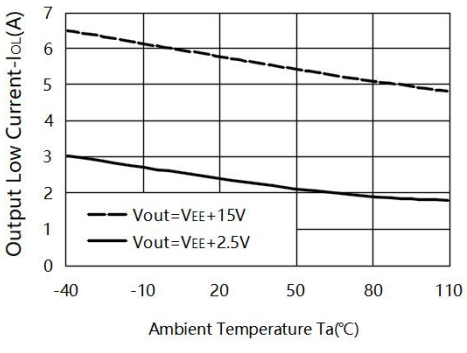


Fig.3 Low Level Output Current During Fault Condition vs. Output Voltage

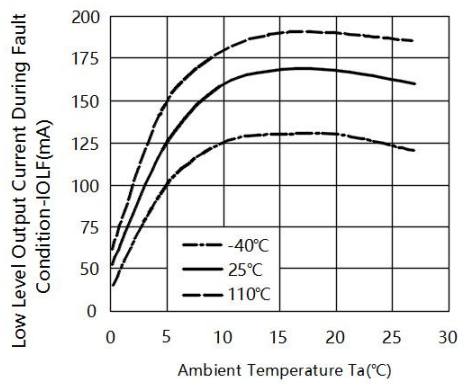


Fig.4 High Output Voltage Drop vs Ambient Temperature

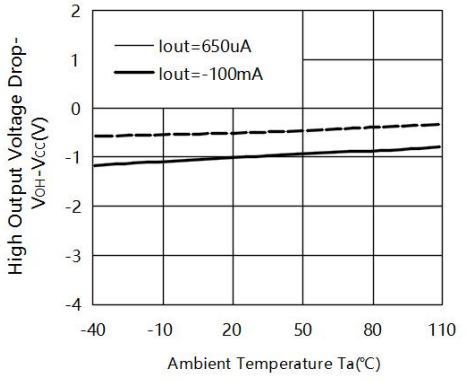


Fig.5 Output Low Voltage vs Ambient Temperature

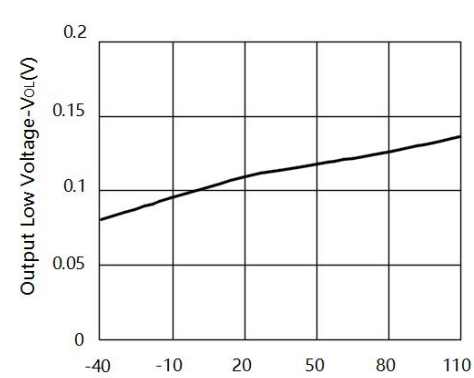


Fig.6 High Output Voltage vs Output High Current

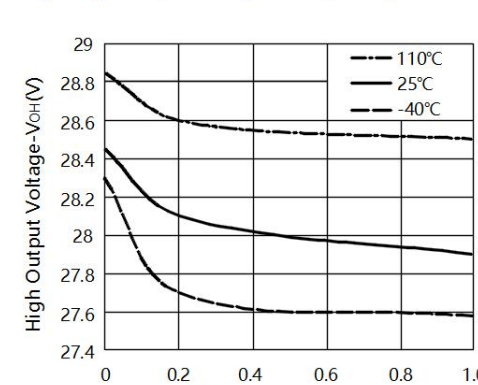


Fig.7 Low Output Voltage vs. Output Low Current

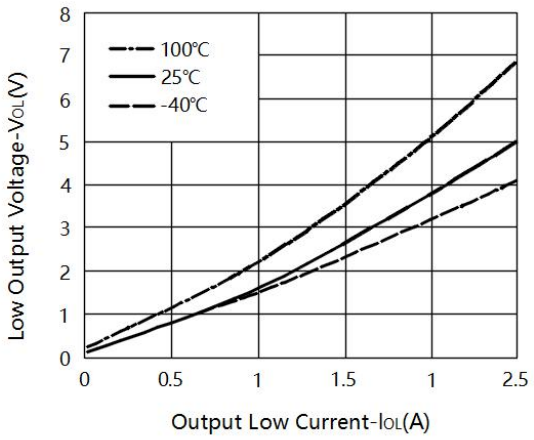


Fig.8 Supply Current vs. Ambient Temperaure

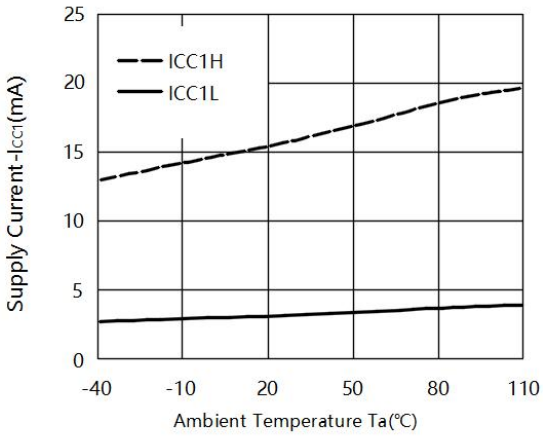


Fig.8 Supply Current vs. Ambient Temperaure

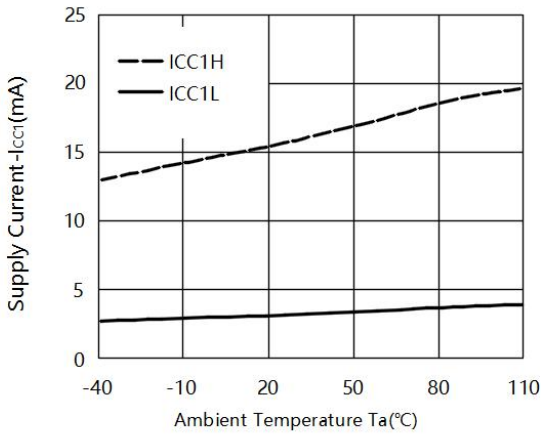


Fig.10 Output Supply Current vs. Output Supply Voltage

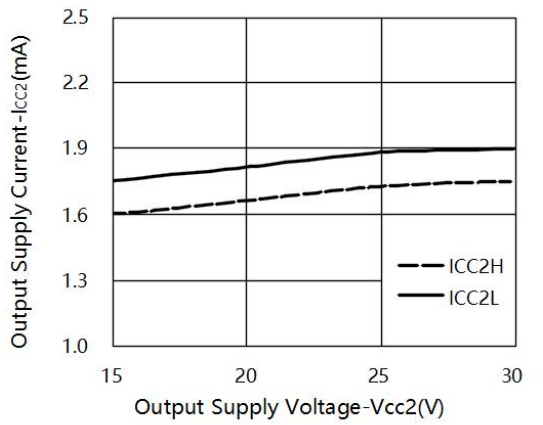


Fig.11 Blanking Capacitor Changing Current vs. Ambient Temperature

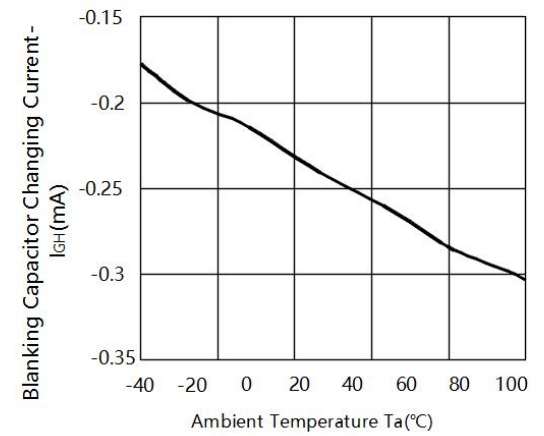


Fig.12 Supply Current vs. Ambient Temperature

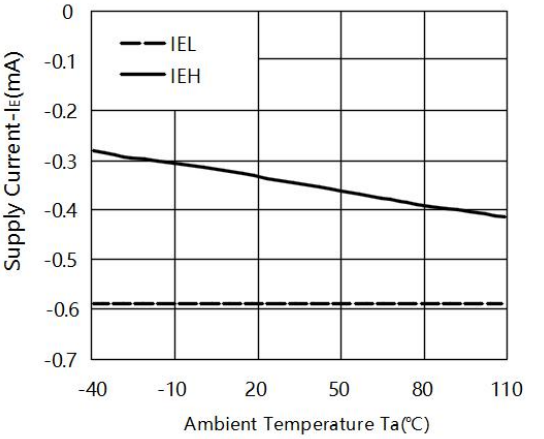


Fig.13 Collector current vs. output current

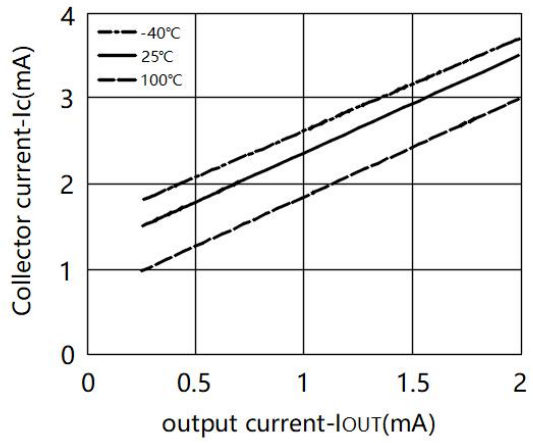


Fig.14 DESAT Threshold vs. Ambient Temperature

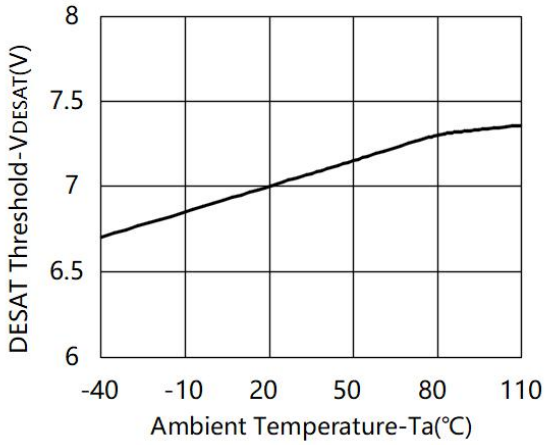


Fig.15 propagation Delay vs. Ambient Temperature

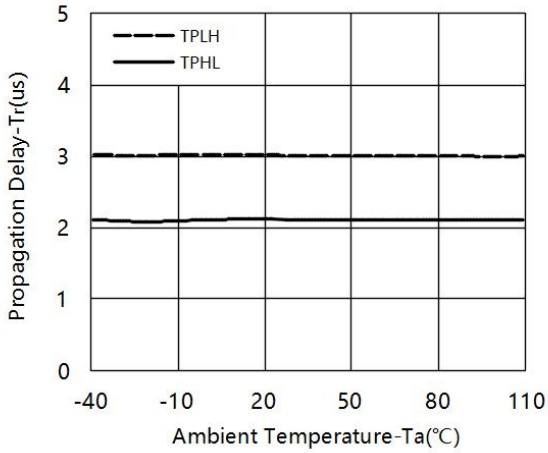


Fig.16 propagation Delay vs. Supply Voltage

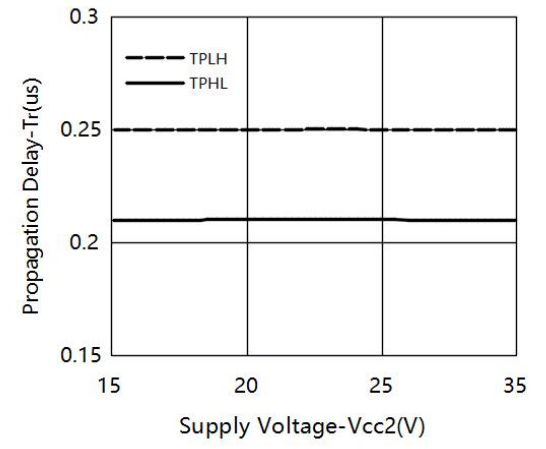


Fig.17 Vin to High propagation Delay vs. Ambient Temperature

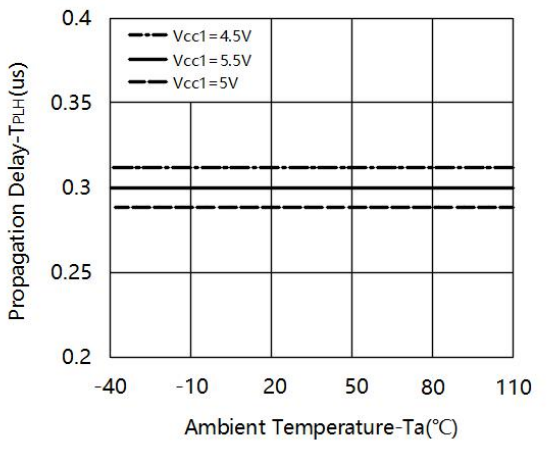


Fig.18 Vin to Low propagation Delay vs. Ambient Temperature

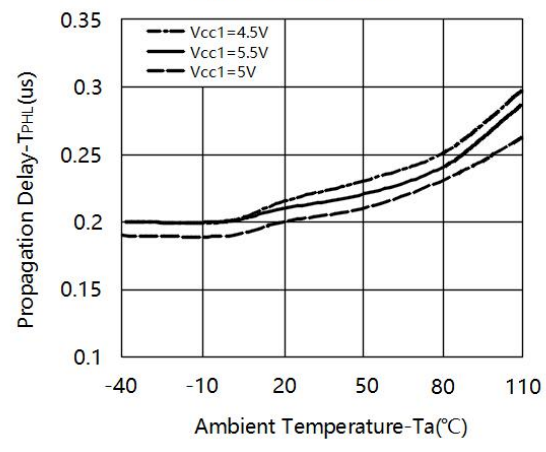


Fig.19 Propagation Delay vs. Load capacitance

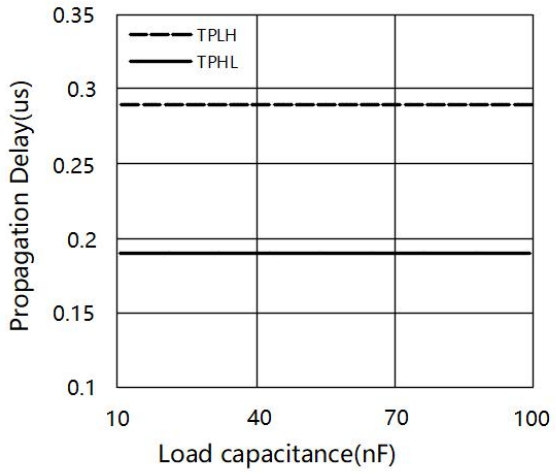


Fig.20 Propagation Delay vs. Load Resistance

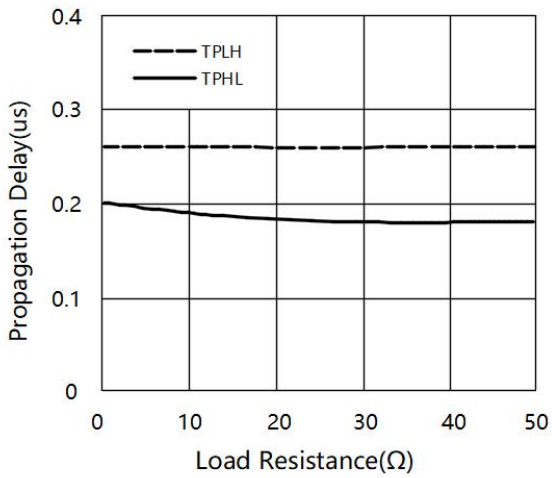


Fig.21 DESAT Sense to 90% Vo Delay vs. Ambient Temperature

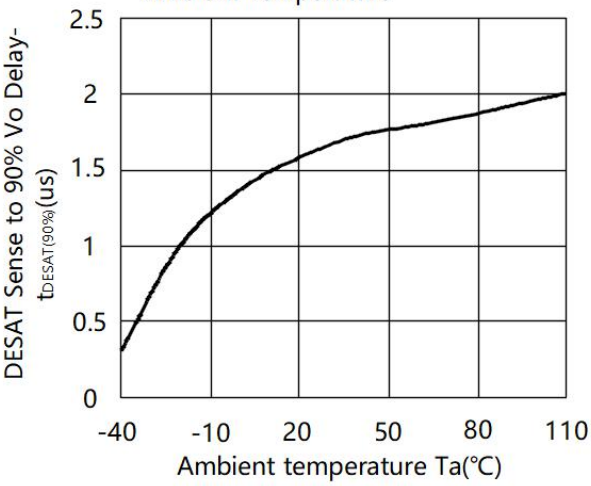


Fig.22 DESAT Sense to 10% Vo Delay vs. Ambient Temperature

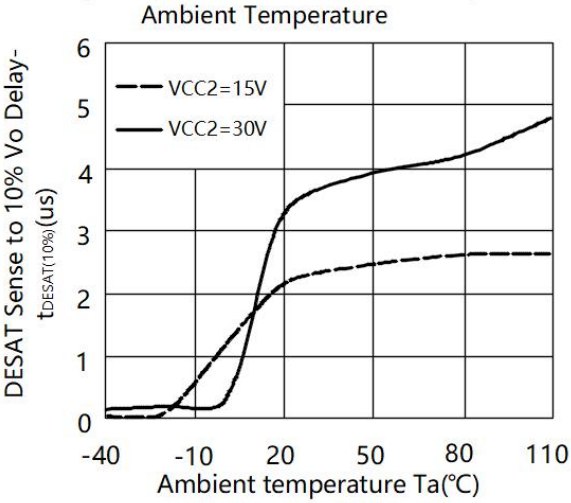


Fig.23 DESAT Sense to 10% Vo Delay vs. Load Capacitance

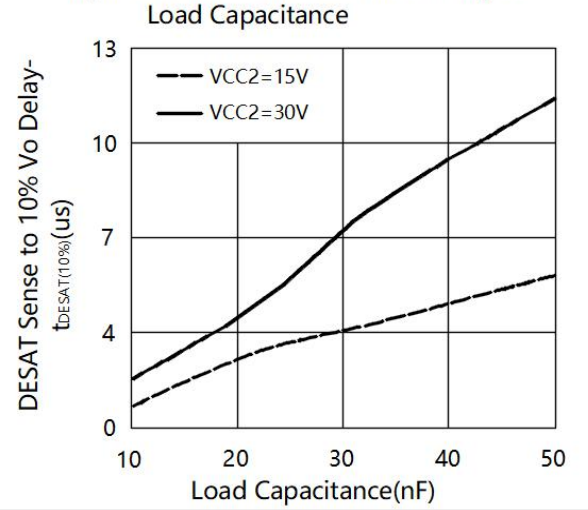
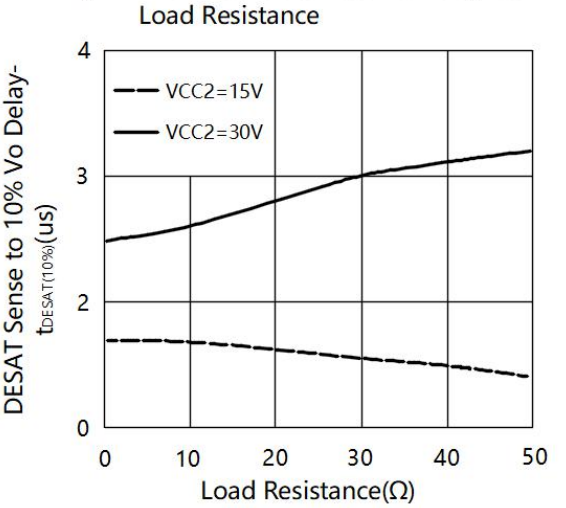


Fig.24 DESAT Sense to 10% Vo Delay vs. Load Resistance



◆ 测试电路图TestCircuits Diagrams

Fig25. $\overline{\text{IFAULTL}}$ test circuit

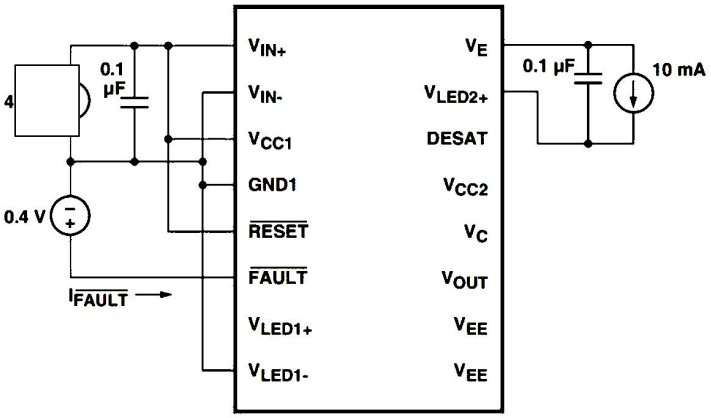


Fig26. $\overline{\text{IFAULTH}}$ test circuit

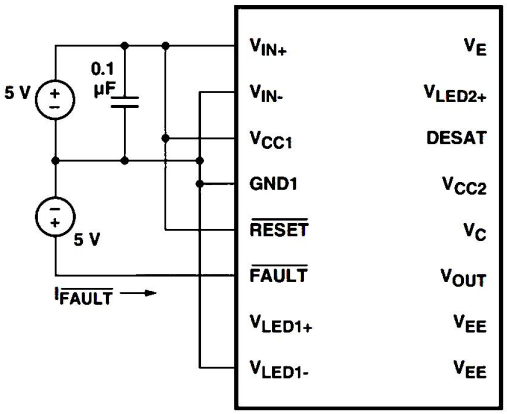


Fig27. IOH Pulsed test circuit

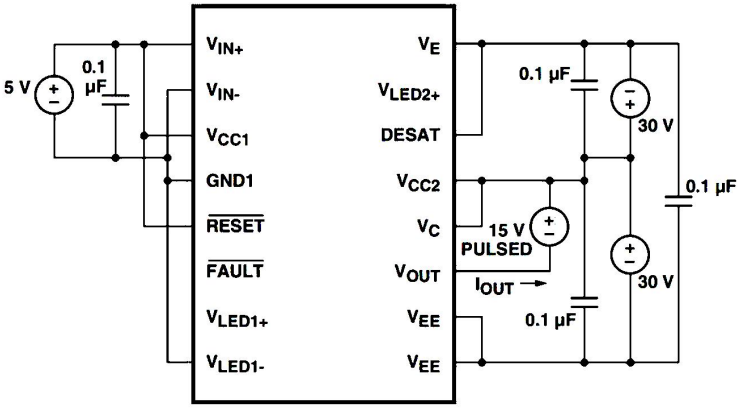


Fig28. IOL Pulsed test circuit

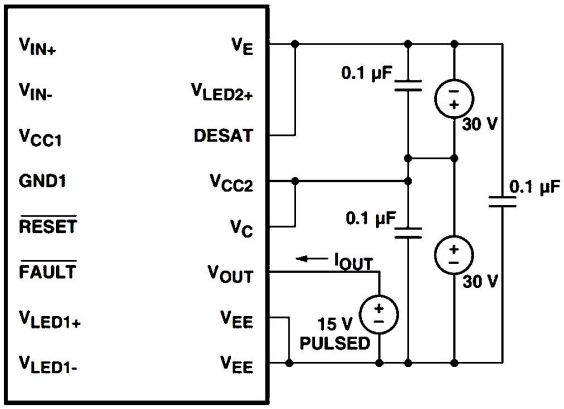


Fig29. IOLF test circuit

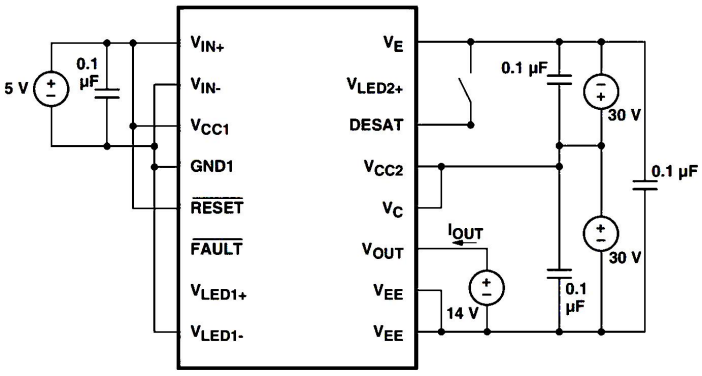


Fig30. VOH Pulsed test circuit

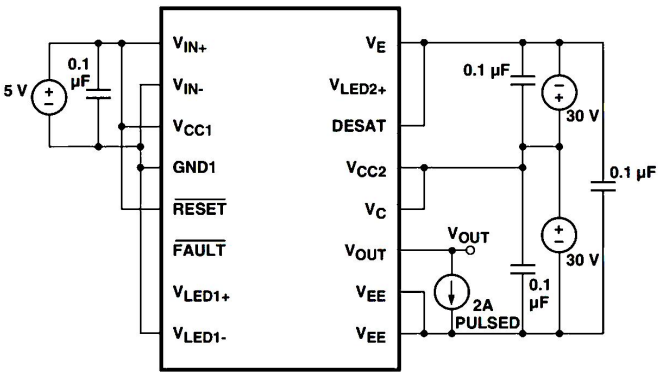


Fig31. VOL test circuit

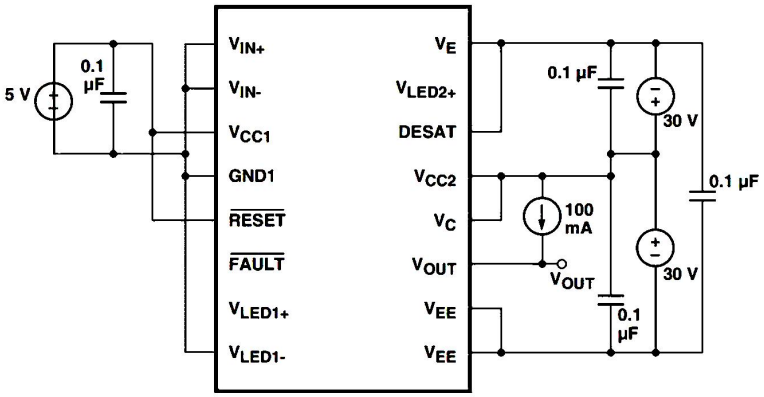


Fig32. ICC1H test circuit

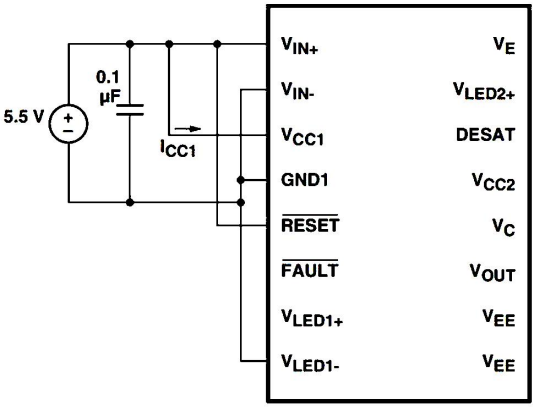


Fig33. ICC1L test circuit

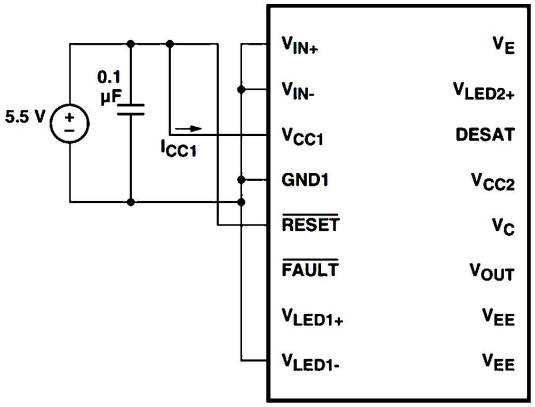


Fig34. ICC2H test circuit

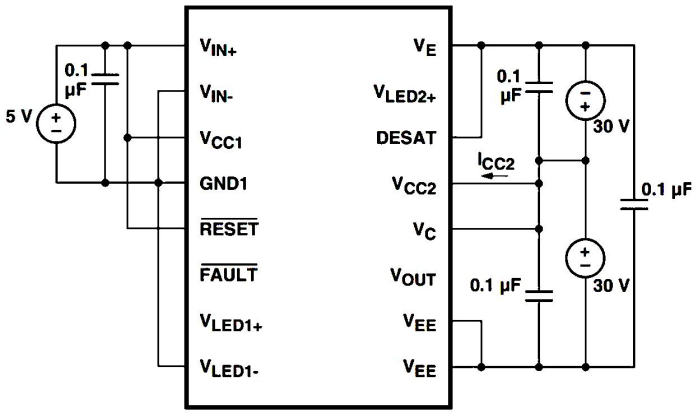


Fig35. ICHG pulsed test circuit

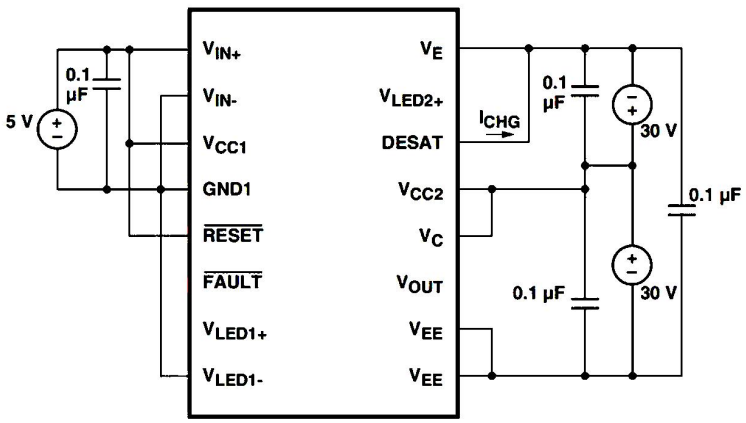


Fig36. ICC2L test circuit

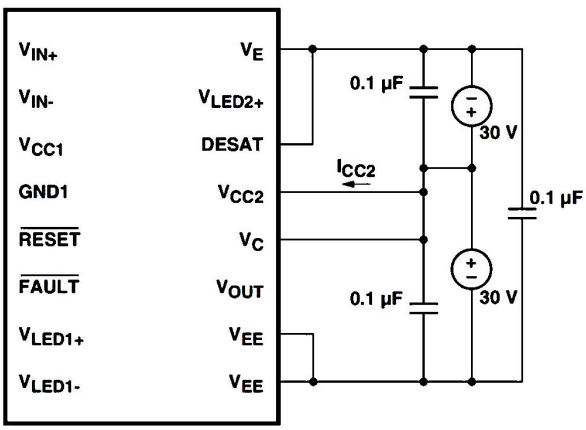


Fig37.UVLO threshold test circuit

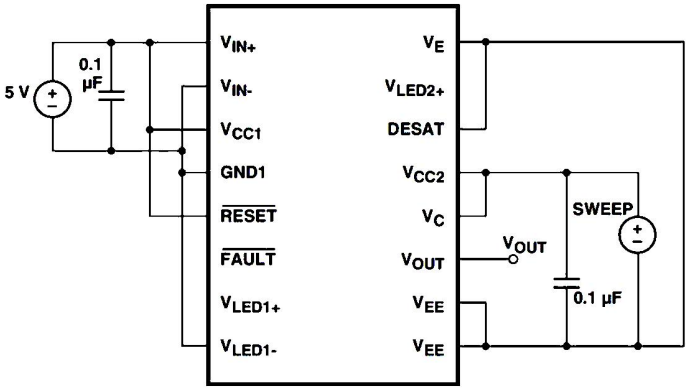


Fig38. I_{DSCHG} test circuit

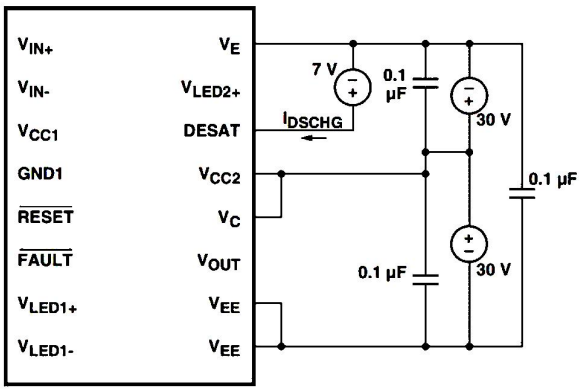


Fig39. DESAT threshold test circuit

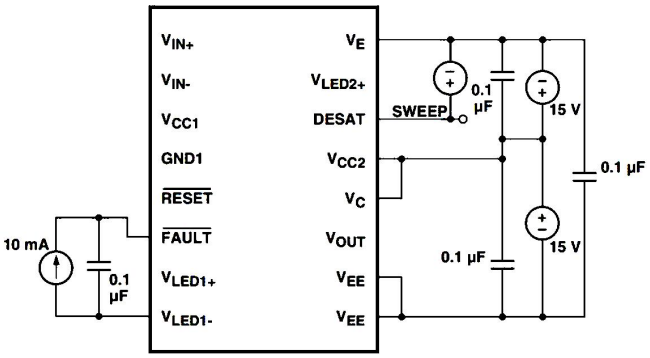


Fig40. T_{PLH} 、T_{PHL}、 Tr 、Tf 、 test circuit

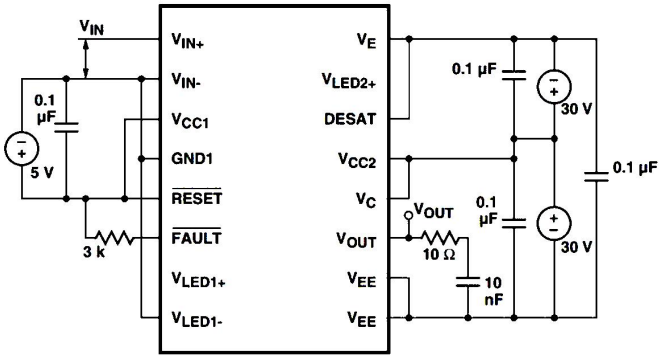


Fig41. $T_{DESAT(10\%)}$ test circuit

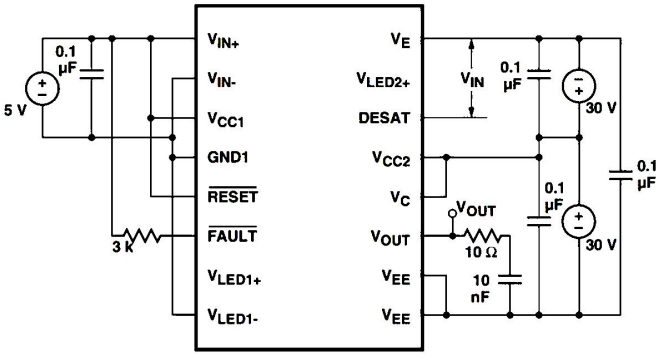


Fig42. $T_{DESAT(FAULT)}$ test

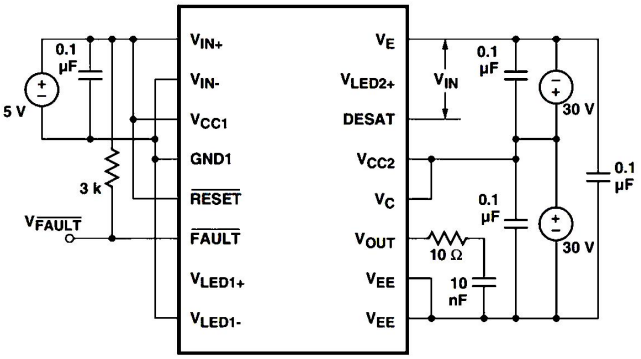


Fig43. $T_{RESET(FAULT)}$ test circuit

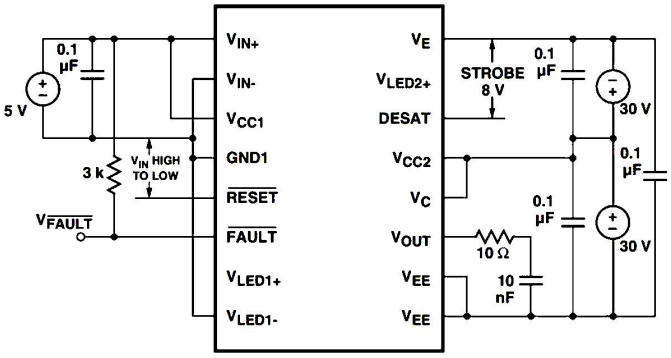


Fig44. UVLO delay test circuit

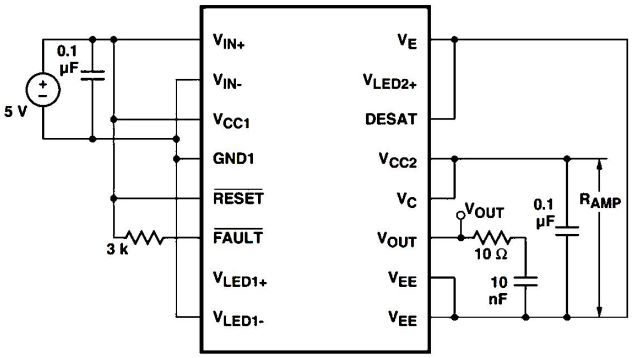


Fig45. CMR test circuit ,LED2 off

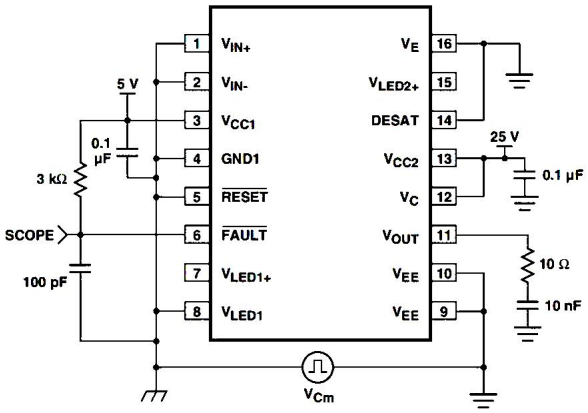


Fig46. CMR test circuit,LED2 on

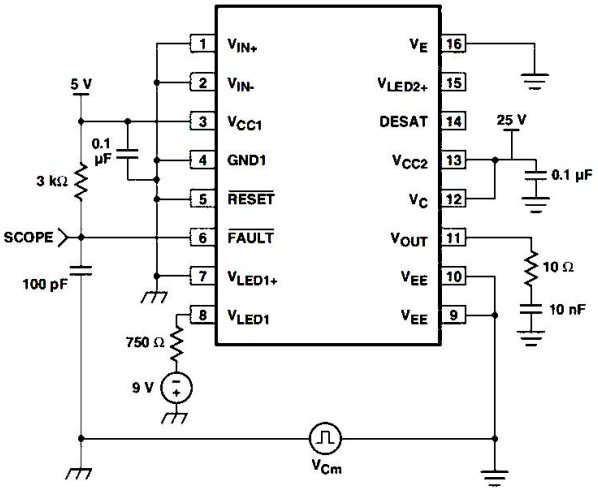


Fig47. CMR test circuit,LED1 off

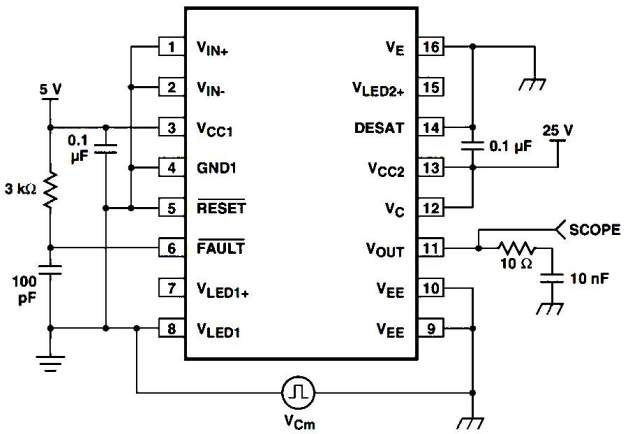


Fig48. CMR test circuit,LED1 on

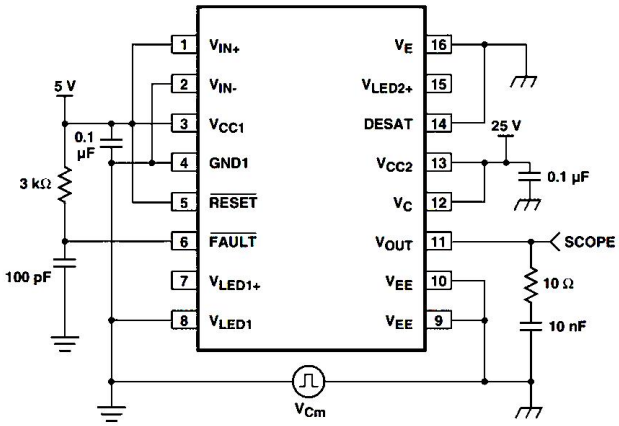


Fig49. ICH test circuit

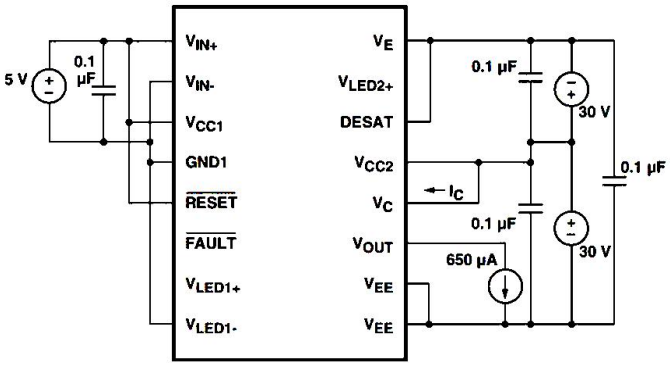


Fig50. ICL test circuit

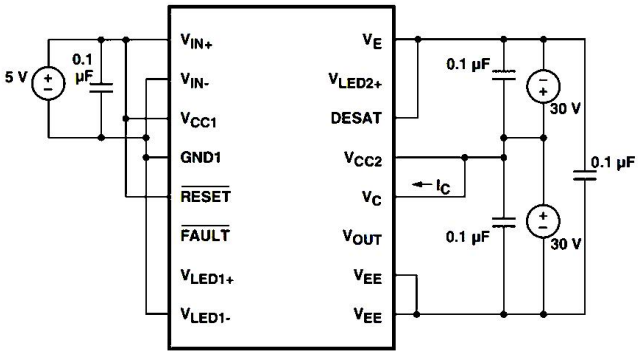


Fig51. I_{EH} test circuit

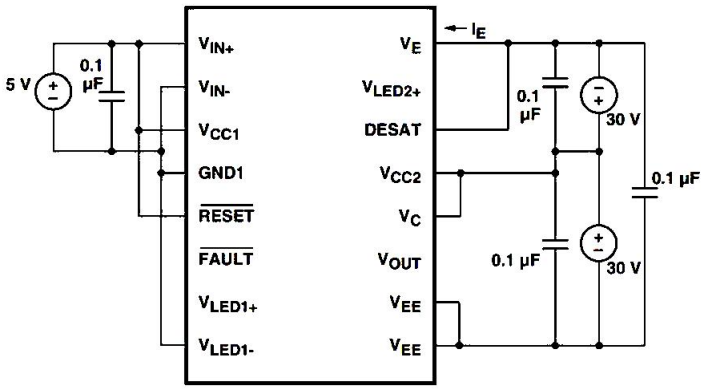


Fig52. I_{CL} test circuit

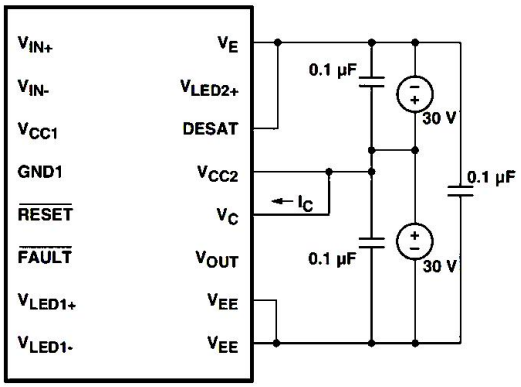


Fig53. I_{EL} test circuit

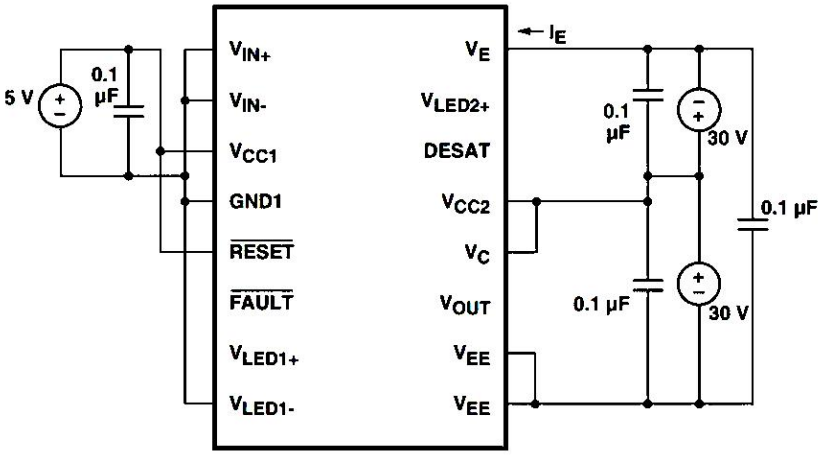


Fig54. VOUT propagation delay wave forms,non inverting configuration

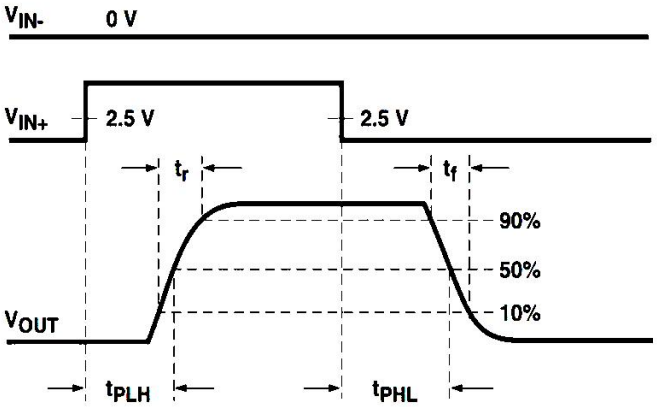


Fig55. VOUT propagation delay wave forms,non inverting configuration

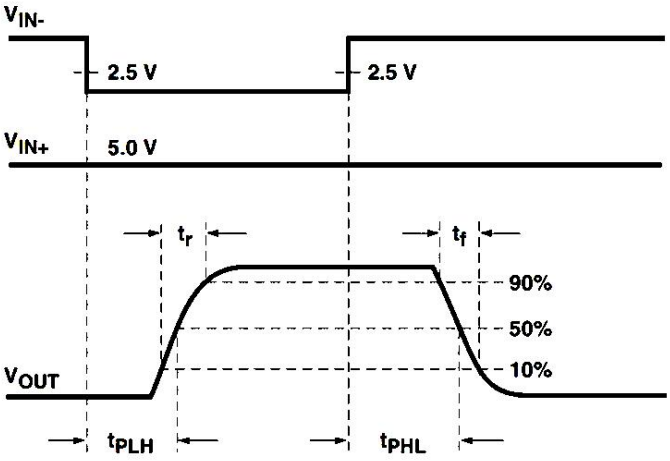
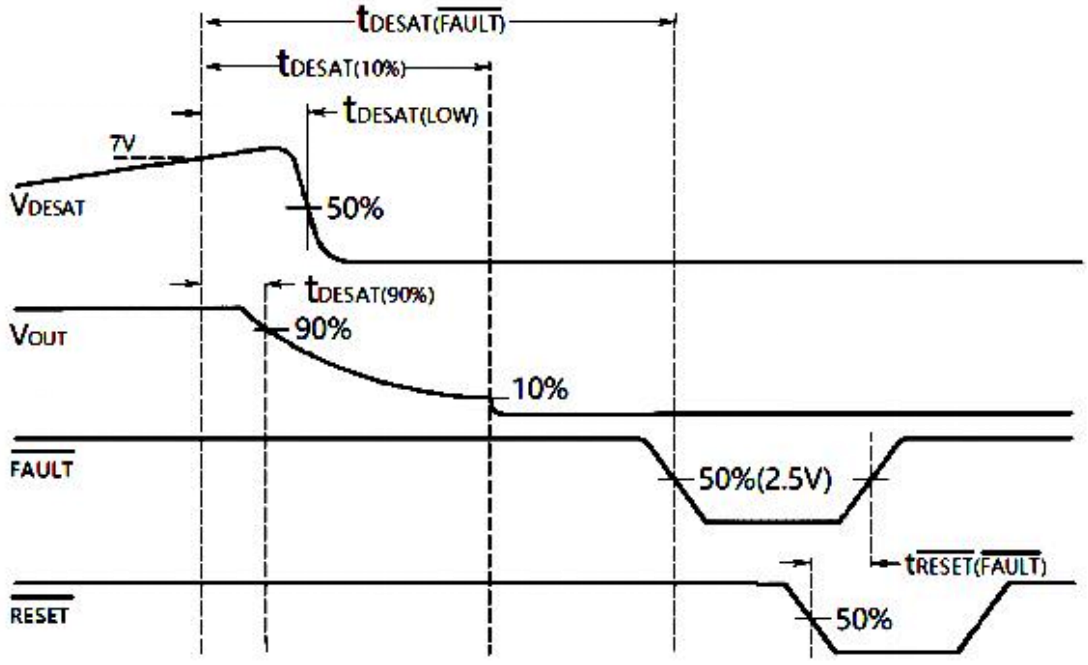


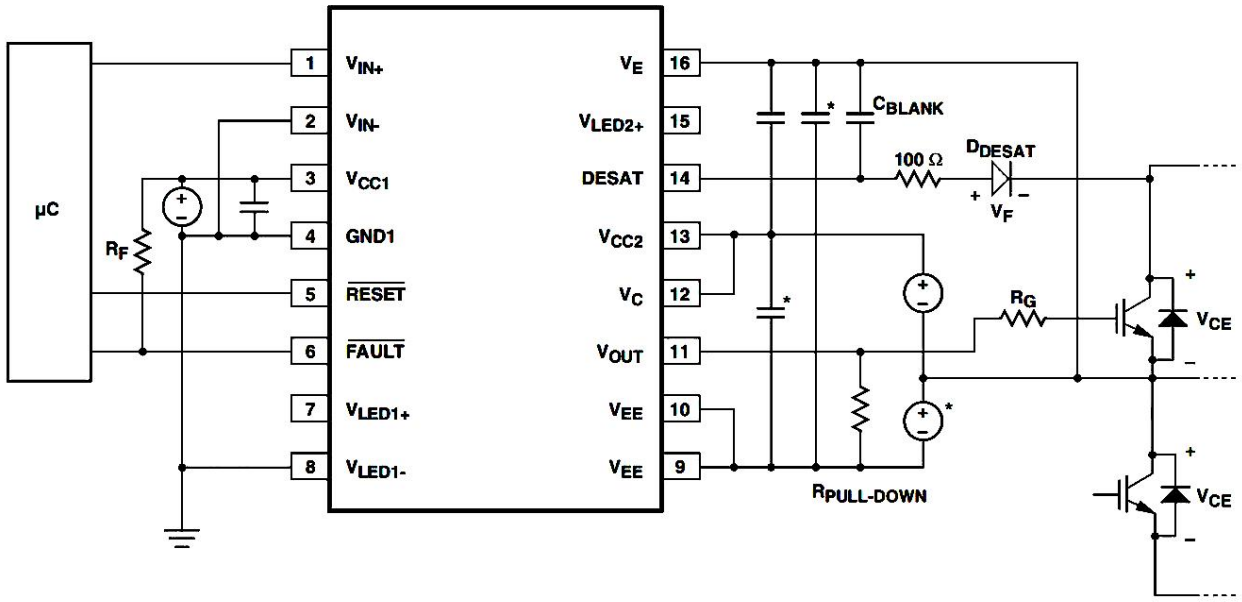
Fig56. DESAT,VOUT,fault,reset delay wave forms.



◆ 典型故障保护IGBT门驱动电路 Typical Fault Protected IGBT Gate Drive Circuit

AT316J 是一款易于使用的智能栅极驱动器， 其IGBT的VCE 故障保护结构紧凑，经济实惠，易于实现。用户可配置输入、集成去饱和VCE 检测、欠压锁定 （UVLO）、IGBT软关断和隔离故障反馈等功能， 以最大限度地提供设计灵活性和电路保护。

The QX316J is an easy-to use, intelligent gate driver which makes IGBT VCE fault protection compact, affordab e, and easy- to-implement. Features such as user configurable inputs, integrated VCE detection, under voltage lockout (UVLO), soft IGBT turn-off and isolated fault feedback provide maximum design flexibility and circuit protection.



1、故障状态下的操作说明 Description of Operation during Fault Condition

DESAT 终端通过 DDESAT 监控 IGBT VCE 电压

DESAT terminal monitors the IGBT VCE voltage through DDESAT.

当 DESAT 端的电压超过 7V 时， IGBT 门电压 （VOUT） 缓慢降低

When the voltage on the DESAT terminal exceeds 7V, the IGBT gate voltage (VOUT) is slowly lowered.

FAULT输出低电平时，通知微控制器故障状态

FAULT output goes low, notifying the microcontroller of the fault condition.

微控制器采取适当的措施

Microcontroller takes appropriate action.

2、输出控制 Output Control

AT316J 的输出(VOUT 和 FAULT)由 VIN, UVLO 和检测到的 IGBT Desat 保护控制。如下表所示 ，AT316J 可以分别使用 VIN+或 VIN-输入来设置反相或非反相。当需要设置反相时，VIN+必须保持在高电平，并切换 VIN-。当需要设置非反相时 ， VIN-必须保持 低电平 ， 并切换 VIN+ 。一旦 UVLO 失效(VCC2 - VE > VUVLO) ，VOUT 被允许输出高电平 ， AT316J 的 DESAT 检测功能将成为 IGBT 保护的主要来源。UVLO 需要确保 DESAT 的功能。一旦 VUVLO+ > 11.6 V, DESAT 持续工作 ， 直到 VUVLO- <12.4 V。因此 ， AT316J 的 DESAT 检测和 UVLO 功能协同工作 ，以确保持续的 IGBT 保护。

The outputs (VOUT and FAULT) of the AT316J are controlled by the combination of VIN, UVLO and a detected IGBT Desat condition. As indicated in the below table, the AT316J can be configured as inverting or non-inverting using the VIN+ or VIN- inputs respectively. when an inverting configuration is desired, VIN+ must be held high and VIN- toggled. when a non-inverting configuration is desired, VIN- must be held low and VIN+ toggled. Once UVLO is not active (VCC2 - VE > VUVLO), VOUT is allowed to go high, and the DESAT detection feature of the AT316J will be the primary source of

IGBT protection. UVLO is needed to ensure DESAT is functional. Once VUVLO+ > 11.6 V, DESAT will remain functional until VUVLO- <12.4V. Thus, the DESAT detection and UVLO features of the AT316J work in conjunction to ensure constant IGBT protection.

VIN+	VIN-	UVLO (VCC2-VE)	Desat condition Detect on Pin14	Pin6 (FAULT) Output	VOUT
X	X	Active	X	X	Low
X	X	X	yes	Low	Low
Low	X	X	X	X	Low
X	High	X	X	X	Low
High	Low	Not Active	No	High	High

◆ 典型的应用和操作 Typical applications and operations

1、故障麻检测与保护技术简介 Introduction to Fault Detection and protection

一个典型的三相逆变器的功率级易发生多种类型的故障 ，其中大多数故障对功率 IGBTs具有潜在的破坏性。这些故障模式 可以分为四种基本类型:由于用户连接错误或线路不良导致的相位或轨道电源短路、由于噪声或计算错误导致的控制信号 故障、由负载引起的过载以及栅极驱动电路中的组件故障。在任何一种故障条件下，通过 IGBTs的电流都会迅速增加，导 致过度的功耗和发热。当负载电流接近器件的饱和电流时 ，IGBTs损坏，并且集电极到发射极的电压上升到饱和电压水平以上。急剧增加的功耗快速令电源设备过热并受到损坏。为了防止损坏驱动器 ，必须实施故障保护，以减少或关闭故障状 态下的过流。

The power stage of a typical three phase inverter is susceptible to several types of failures, most of hich are potentially destructive to the power IGBTs. These failure modes can be grouped into four basic categories: phase and/or rail supply short circuits due to user misconnect or bad wiring, control signal failures due to noise or computational errors, overload conditions induced by the load, and component failures in the gate drive circuitry. under any of these fault conditions, the current through the IGBTs can increase rapidly, causing excessive power dissipation and heating. The IGBTs become damaged when the current load approaches the saturation current of the device, and the collector to emitter voltage rises above the saturation voltage level. The drastically increased power dissipation very quickly overheats the power device and destroys it. To prevent damage to the drive, fault protection must be implemented to reduce or turn-off the overcurrents during a fault condition.

一种理想的解决方案就是提供快速的本地故障检测和关闭的电路 ，但迄今为止，所需的元件数量 ，电路板空间的消耗 ， 成本和复杂性限制了其在高性能驱动器中的使用。该电路必须具有高速、低成本、低分辨率、低功耗和体积小的特点。 A circuit providing fast local fault detection and shutdown is an ideal solution, but the number of required compon- ents, board space consumed, cost, and complexity have until now limited its use to high performance drives. The features which this circuit must have are high speed, low cost, low resolution, low power dissipation, and small size.

2、应用程字信息Application Word Information

AT316J 满足了将高速、大电流输出驱动器、输入和输出之间的高压光隔离、IGBT 饱和检测、关断以及一个光隔离的故障 状态信号反债集成到一个 16 引脚封装中的标准。

The AT316J satisfies these criteria by combining a high speed, high output current driver, high voltage optical isolation between the input and output, local IGBT desaturation detection and shutdown, and an optically isolated fault status feedback signal into a single 16-pin surface mount package.
AT316J 中采用的故障检测方法是通过监测IGBT的饱和(集电极）电压，并在集电极电压超过预定國值时触发局部故障停 机而实现的。小栅极放电装置缓慢降低由 IGBT 短路引起的大电流，防止产生破坏性尖峰电压。在能耗达到破坏性水平之前 ，将IGBT关断。在IGBT关断状态期间，故障检测电路失效，以防止产生虚假的故障”信号。
The fault detection method, which is adopted in the AT316J, is to monitor the saturation (collector) voltage of the IGBT and to trigger a local fault shutdown sequence if the collector voltage exceeds a predetermined threshold. A small gate discharge device slowly reduces the high short circuit IGBT current to prevent damaging voltage spikes. Before the dissipated energy can reach destructive levels, the IGBT is shut off. During the off state of the IGBT, the fault detect circuitry is simply disabled to prevent false ,fault,signals.
如果功率器件的短路能力已知 ，有效的替代保护方案是测量 IGBT 电流以防止去饱和 ，但是如果栅极驱动电压降低到仅能 将 IGBT 部分接通 ，则该方法将失败。通过直接测量集电极电压 ，AT316J 即使在栅极驱动电压不足的情况下也能限制 IGBT 的功耗。去饱和检测方法的另一个更巧妙的优势是监控 IGBT 的功耗 ，采用电流感测法 ，预设一个电流國值来预测安 全工作的范围。因此 ，不需要过于保守的过电流國值来保护 IGBT。
The alternative protection scheme of measuring IGBT current to prevent desaturation is effective if the short circuit capability of the power device is known, but this method will fail if the gate drive voltage decreases enough to only partially turn on the IGBT. By directly measuring the collector voltage, the AT316J limits the power dissipation in the IGBT even with insufficient gate drive voltage. Another more subtle advantage of the desaturation detection method is that power dissipation in the IGBT is monitored, while the current sense method relies on a preset current threshold to predict the safe limit of operation. Therefore, an overly conservative over current threshold is not needed to protect the IGBT.

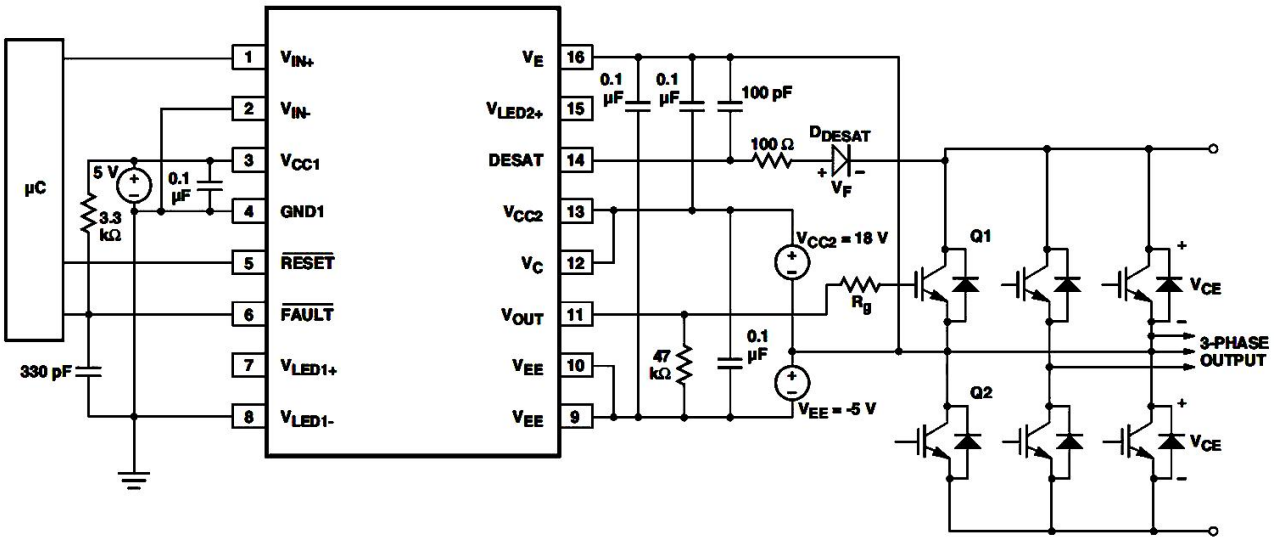
3、推荐应用电路Recommended Application circuit

AT316J 具有反相和非反相栅极控制输入 ，一个有源低电平复位输入和一个开路集电极故障输出 ，适用于“或”逻辑电路应 用。图 57 中所示的推荐应用电路体现了使用 AT316J 的典型栅极驱动电路。
The AT316J has both inverting and non-inverting gate control inputs, an active low reset input, and an open collector fault output suitable for wired ,OR,applications. The recommended application circuit shown in Figure 57 illustrates a typical gate drive implementation using the AT316J.

四个电源旁路电容器(0.1μF)在开关瞬态提供瞬态大电流。由于充电电流的瞬态性质 ，一个小功率电流(5mA)电源就足够了。DESAT 二极管和 100pF 的电容是故障检测电路中必不可少的外部元件。栅极电阻(10Ω)用于限制栅极充电电流，并控制IGBT集电极电压的上升和下降时间。开路集电极故障输出有一个无源上拉电阻 3.3kΩ和一个330pF 的滤波电容。VOUT的47kΩ下拉电阻可提供一个可预测的高电平输出电压(VOH)。在这类应用中，当检测到故障时，IGBT门驱动器将关断，直到微控制器施加复位信号后才会恢复开启。
The four supply bypass capacitors (0.1 μF) provide the large transient currents necessary during a switching transition. Because of the transient nature of the charging currents, a low current (5mA) power supply suffices. The DESAT diode and 100pF capacitor are the necessary external components for the fault detection circuitry. The gate resistor (10Ω) serves to limit gate charge current and indirectly control the IGBT collector voltage rise and fall times. The open collector fault output has a passive 3.3kΩ pull-up resistor and a 330 pF filtering capacitor. A 47kΩ pulldown resistor on VOUT provides a more predictable high level output voltage (VOH). In this application, the IGBT gate driver will shut

down when a fault is detected and will not resume switching until the microcontroller applies a reset signal.

Fig57. Recommended application circuit



◆ 行为电路示意图Behavioral Circuit Diagram

AT316J 的功能行为由图60中的逻辑图表示，该逻辑图充分描述了AT316J内部和外部信号的相互作用和序列。
The functional behavior of the AT316J is represented by the logic diagram in Figure 60 which fully describes the interaction and sequence of internal and external signals in the AT316J.

1、输入INPUT

在正常开关模式下，未检测到输出故障，故障锁存器的低状态允许输入信号控制LED信号。故障输出处于集电极开路状态，复位引脚的状态不影响对IGBT栅极的控制。当检测到故障时，故障输出和信号输入都被锁存。故障输出变为低电平 有效状态，信号LED被强制关端输出低电平)。锁存状态将持续存在，直至复位引脚被拉低为止。
In the normal switching mode，no output fault has been detected，and the low state of the fault latch allows the input signals to control the signal LED. The fault output is in the open-collector state，and the state of the Reset pin does not affect the control of the IGBT gate. when a fault is detected，the FAULT output and signal input are both latched. The fault output changes to an active low state，and the signal LED is forced off（output LOw). The latched condition will persist until the Reset pin is pulled low.

2. 输出OUTPUT

三个内部信号控制驱动器输出的状态: LED信号的状态 ，UVLO和故障信号。如果IGBT集电极未检测到故障 ，且供电电压高于UVLO國值，则LED信号将控制驱动器的输出状态。逻辑驱动器中有一个互锁装置，以确保输出级的上拉和下拉 装置永远不会同时导通。如果检测到欠压状态，无论LED状态如何，输出将被50x DMOS设备主动拉低。如果在LED信号亮起时检测到IGBT去饱和故障 ，故障信号将被锁存在高电平状态。三重达林顿和 50x DMOS设备被禁用，一个较小的 1x DMOS下拉设备被激活，缓慢地对IGBT栅极放电。当输出降至2V以下时 ，50x DMOS设备再次开启 ，将IGBT栅 极牢牢地钳位在VEE上。故障信号仍保持锁存在高电平状态 直到LED信号关断。
Three internal signals control the state of the driver output: the state of the signal LED，as well as the UVLO and Fault signals. If no fault on the IGBT collector is detected，and the supply voltage is above the UVLO threshold，the LED signal will control the driver output state. The driver stage logic includes an interlock to ensure that the pull-up and pull-down devices in the output stage are never on at the same time. If an undervoltage condition is detected，the output will be actively pulled low by the 50x DMOS device，regardless of the LED state. If an IGBT desaturation fault is detected while the signal LED is on，the Fault signal will latch in the high state. The triple darlington AND the 50x DMOS device are disabled

，and a smaller 1x DMOS pull-down device is activated to slowly discharge the IGBT gate. when the output drops below two volts，the 50x DMOS device again turns on，clamping the IGBT gate firmly to VEE. The Fault signal remains latched in the high state until the signal LED turns off.

Fig58. Behavioral Circuit Schematic

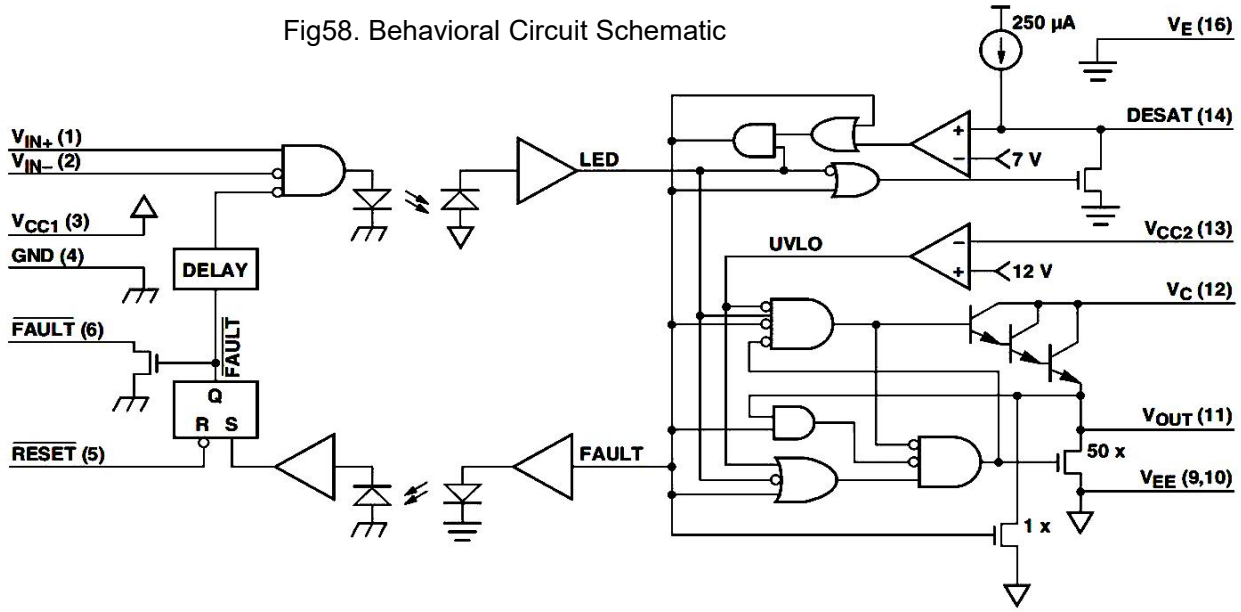
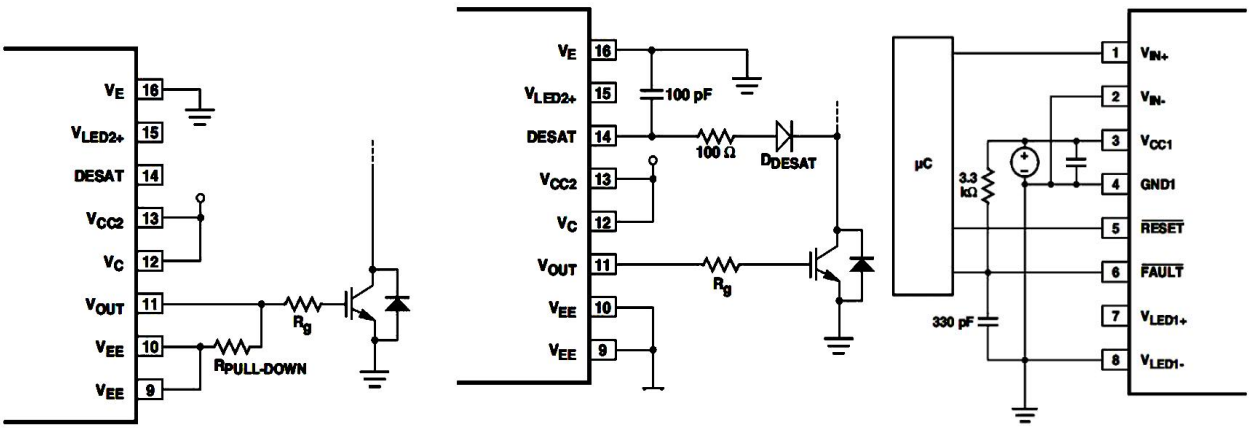


Fig59. Output pull-down resistor Fig60. DESAT pin protection Fig61. FAULT pin CMR protection



3、其他推存的组件 Other recommended components

图 57 中的应用电路包括一个输出下拉电阻、一个 DESAT 引脚保护电阻、一个 FAULT 引脚电容(330pF)和一个 FAULT 引 脚上拉电阻。

The application circuit in Figure 57 includes an output pull-down resistor, a DESAT pin protection resistor, a FAULT pin capacitor (330pF), and a FAULT pin pull-up resistor.

4、输出下拉电器。Output pull - Down Resistor

在输出为高电平的转换期间 ,输出电压迅速上升至 VCC2 ,并保持在 3 个二极管压降以内。如果输出电流因容性负载而降至 零 ,输出电压将在几微秒内缓慢上升约至 VCC2 -3(VBE)与 VCC2 之间。为了将输出电压限制在 VCC2 -3(VBE) ,建议在输出端与 VEE 之间接一个下拉电阻 RPULL-DOWN ,以便在输出为高电平时产生几个 650μA 的灌电流。下拉电阻值取决于正向电源的值 ，可以根据公式 Rpull-down =[VCC2 -3 *(VBE)]/650 μA 进行调整。

During the output high transition, the output voltage rapidly rises to within 3 diode drops of VCC2 . If the output current then drops to zero due to a capacitive load, the output voltage will slowly rise from roughly VCC2 -3(VBE) to VCC2 within a period of several microseconds. To limit the output voltage to VCC2 -3(VBE), a pull-down resistor, RPULL- DOWN between the output and VEE is recommended to sink a static current of several 650μA while the output is high. Pull-down resistor values are dependent on the amount of positive supply and can be adjusted according to the formula, Rpull-down = [VCC2 -3 * (VBE)] / 650μA.

5、DESAT引脚保护DESAT pin protection

与 IGBTs连接的续流二极管会产生大大超过二极管正向电压理论值的瞬态正向电压。这可能会导致DESAT引脚上产生较 大的反向尖峰电压，如果不采取保护措施的话 ，将从集成电路中转移大量电流。为了将这个电流限制在不会损坏集成电路的水平 ，需要插入一个100欧姆的电阻与DESAT二极管串联。这个新增的电阻不会改变 DESAT 國值或DESAT消隐时间。

The freewheeling of fly back diodes connected across the IGBTs can have large instantaneous forward voltage transients which greatly exceed the nominal forward voltage of the diode. This may result in a large negative voltage spike on the DESAT pin which will draw substantial current out of the IC if protection is not used. To limit this current to levels that will not damage the IC, a 100 ohm resistor should be inserted in series with the DESAT diode. The added resistance will not alter the DESAT threshold or the DESAT blanking time.

6、高CMR的FAULT引脚上的电容 capacitance FAULT pin for High CMR

当故障输出处于高状态时，快速共模瞬态会影响故障端电压。故障端和地之间应连接一个330pF电容器(图 60)，当额定 CMR为15kV/ μs 时，可获得足够的CMOS 声容限。当检测到去饱和状态时，新增的电容不会增加故障输出延迟。

Rapid common mode transients can affect the fault pin voltage while the fault output is in the high state. A 330pF capacitor（Fig. 60) should be connected between the fault pin and ground to achieve adequate CMOS noise margins at the specified CMR value of 15kV/μs. The added capacitance does not increase the fault output delay when a desaturation condition is detected.

7、FAULT引脚上的上拉电阻器pull-UP Resist or on FAULT pin

故障引脚是一个集电器开路输出 ，因此需要一个上拉电阻来提供高电平信号。

The FAULT pin is an open-collector output and therefore requires a pull-up resistor to provide a high-level signal.

8、对于高CMR，采用标准的CMOS或TTL驱动电路Driving with standard CMOS/TLfor High CMR

从隔离式高压电路到输入端涉及到的电路的电容糯合是 CMR 的主要限制。必须考虑到这种糯合 ，以实现较高的 CMR 性 能。输入引脚 VIN+和 VIN-必须有自启动信号 ，以防止在极端共模瞬态条件下输出的意外切换。应避免使用上拉或下拉电阻 的输入驱动电路 ，如集电极开路结构。建议使用标准的 CMOS 或 TTL 驱动电路

Capacitive coupling from the isolated high voltage circuitry to the input referred circuitry is the primary CMR limitation. This coupling must be accounted for to achieve high CMR performance. The input pins VIN+ and VIN- must have active drive signals to prevent unwanted switching of the output under extreme common mode transient conditions. Input drive circuits that use pull-up or pull-down resistors, such as open collector configurations, should be avoided. Standard CMOS or TTL drive circuits are recommended

9、AT316J输入端的用户配量user-configurationottheAT316JInputside

VIN+ ,VIN- ,FAULT 和 RESET 输入引脚令各种栅极控制和故障配置成为可能 ，具体取决于电机驱动要求。AT316J 同时具有反相和非反相栅极控制输入,适用于“或”应用的集电极开路故障输出和自动低电平复位输入。

The VIN+, VIN-, FAULT and RESET input pins make a wide variety of gate control and fault Configurations possible,depending on the motor drive requirements. The AT316J has both inverting and noninverting gate control inputs, an open collector fault output suitable for wired，OR,applications and an active low reset input.

Figure 62. Typical input configuration, noninverting

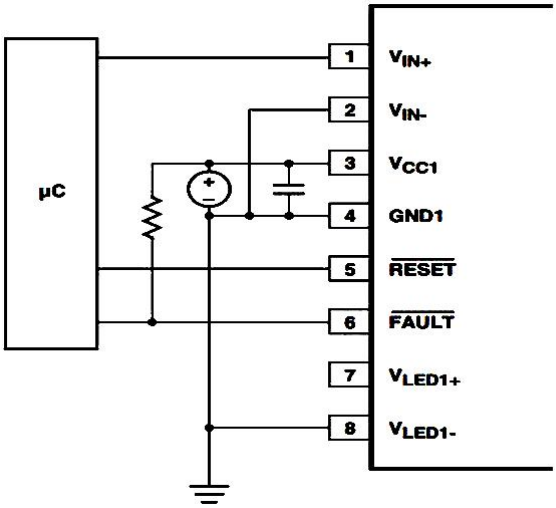


Figure 63. Typical Input configuration, Inverting

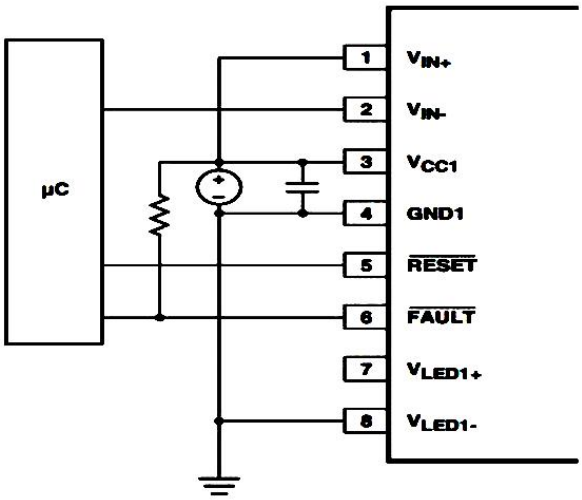
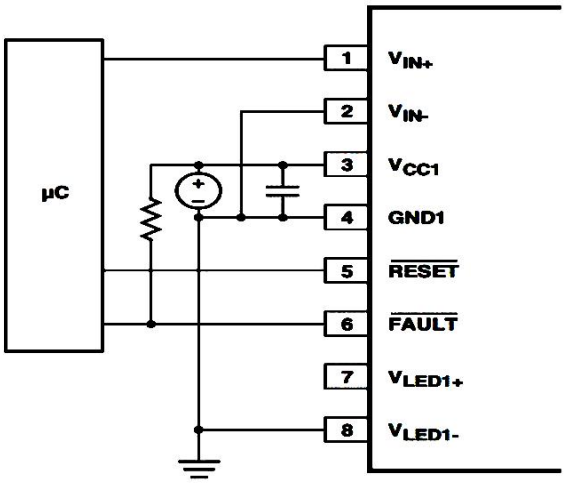


Figure 64. Local shutdown, local reset configuration



10、AT316J非反相反相模式动输入DrivingInputpfA316JinNon-inverting/Inverting Mode

AT316J 的栅极驱动电压输出可以使用VIN-和VIN+输入来设置反相或非反相。如图62所示 ,当需要设置非反相时 ,通过将其连接到 GND1 ,将 VIN-保持在低电平 ,并切换 VIN+。如图63所示 ,当需要设置反相时 ,VIN+连接到 Vcc1 ,其保持在高 电平 ,并切换 VIN- 。

The Gate Drive Voltage Output of the AT316J can be configured as inverting or non-inverting using the VIN- and VIN+ inputs. As shown in Figure 62, when a non-inverting configuration is desired, VIN- is held low by connecting it to GND1 and VIN+ is toggled. As shown in Figure 63, when an inverting configuration is desired, VIN+ is held high by connecting it to Vcc1 and VIN- is toggled.

11、局部关断，局部复位Local shutdown,Local Reset

如图 64 所示 ,对 AT316J 栅极驱动器的故障输出分别进行轮询 ,并且在故障发生后 ,独立断定复位线为低电平 ,从而复位电机控制器。

As shown in Figure 64, the fault output of each AT316J gate driver is polled separately, and the individual reset lines are asserted low independently to reset the motor controller after a fault condition.

12、全部关断，全部复位Global-shutdown,Global Reset

如图65所示，当设置为反相操作时，通过将 FAULT 输出绑定到VIN+ ，可以将 AT316J 设置为在故障情况下自动关断。对于高可靠性的驱动器 ，每个AT316J的集电器开路故障输出可以在一个共同的故障总线上连接在一起 ，形成一个单独的 故障总线直接与微控制器接口。当6 栅极驱动器中的任何一个检测到故障时 ， 故障输出信号将同时禁用这6个AT316J栅极驱动器，从而防止产生进一步的灾难性故障。

As shown in Figure 65, when configured for inverting operation, the AT316J can be configured to shutdown automatically in the event of a fault condition by tying the FAULT output to VIN+. For high reliability drives, the open collector FAULT outputs of each AT316J can be wire ,OR,ed together on a common fault bus, forming a single fault bus for interfacing directly to the micro-controller. When any of the six gate drivers detects a fault, the fault output signal will disable all six AT316J gate drivers simultaneously and thereby provide protection against further catastrophic failures.

Figure 65. Global-shutdown, global reset configuration

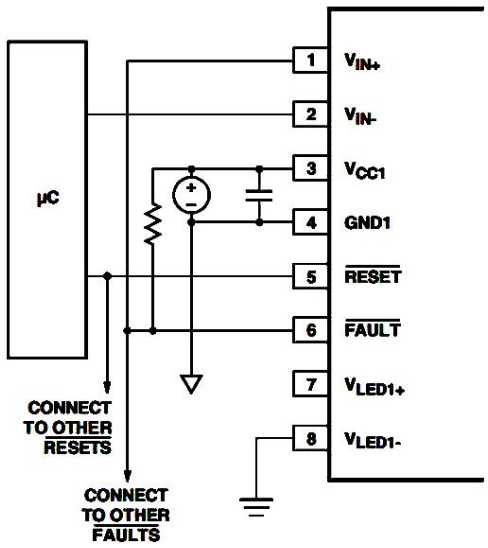


Figure 66. Auto-reset configuration

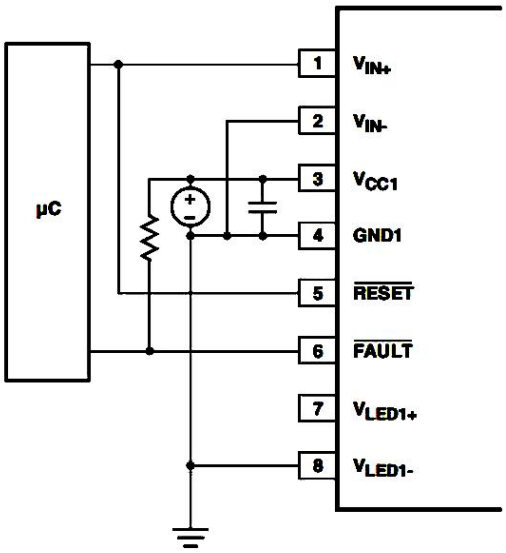


Figure 67a. safe hardware reset for noninverting input configuration (automatically resets for every

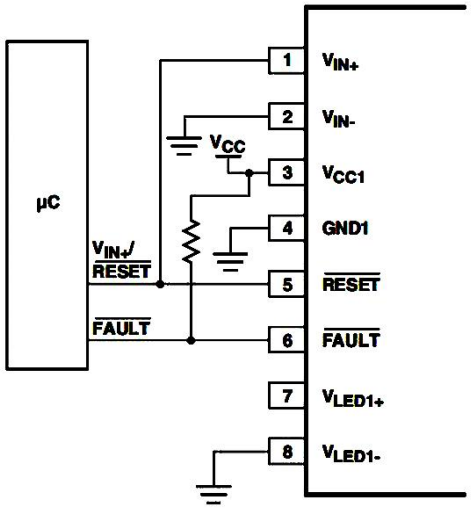
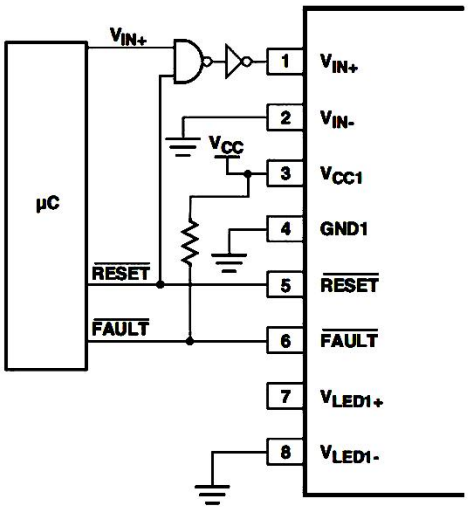


Figure 67b. safe hardware reset for noninverting input configuration



13、自动复位Auto-Reset

如图66所示，当反相VIN-输入连接到地面(设置非反相）时 ，通过将 RESET 连接VIN+ ，可以将AT316J设置为自动复位。在这种情况下，在这种情况下，每个开关周期对非反相输入端和复位输入端施加栅极控制信号来复位故障锁存器。在IGBT 正常工作时 ，断定复位输入低电平无效。发生故障后，门极驱动器保持在锁存故障状态，直到栅极控制信号变为写门 低写状态并重置故障锁存。如果门极控制信号为连续的PW M信号，则故障锁存器在下一次输入信号变高时将一直复位。

这种配置在逐周期的基础上保护 IGBT，并在下一个写开启写周期之前自动复位。故障输出可以通过连接写 OR 写来提醒微控制 器 ，但在这种(自动复位)配置下，该信号不能用于控制目的。此配置会逐个循环地保护IGBT ，并在下一个“开启”循环之前自动重置。故障输出可以连接起来或一起提醒微控制器，但这个信号不会用于此(自动重置）配置中的控制目的。当AT316J设置为自动复位时，保证的最小故障信号脉冲宽度为3μs。

As shown in Figure 66, when the inverting VIN- input is connected to ground (non-inverting configuration), the AT316J can be configured to reset automatically by connecting RESET to VIN+ . In this case, the gate control signal is applied to the non-inverting input as well as the reset input to reset the fault latch every switching cycle. Duringnormal operation of the IGBT, asserting the reset input low has no effect. Following a fault condition, the gate driver remains in the latched fault state until the gate control signal changes to the ,gate low,state and resets the fault latch. If the gate control signal is a continuous PWM signal, the fault latch will always be reset by the next time the input signal goes high. This configuration protects the IGBT on a cycle-by-cycle basis and automatically resets before the next ,on,cycle. The fault outputs can be wire ,OR,ed together to alert the micro- controller, but this signal would not be used for control purposes in this (Auto-Reset) configuration. When the AT316J is configured for Auto-Reset, the guaranteed minimum FAULT signal pulse width is 3 μs.

14、遵循故障条件进行重置Resetting Following Fault condition

为了在故障状态(FAULT 输出低电平）后恢复正常的开关操作 ，RESET引脚必须输出为低电平，以释放内部故障锁存器并重置FAULT输出(高电平）。在确定RESET管脚为低电平之前 ，输入(VIN ）开关信号必须设置为输出(VOL ）低电平状态。这可以通过微控制器直接处理，也可以通过硬连线将RESET信号与合适的输入信号进行同步。这可以通过微控 制器直接处理 ，也可以通过硬连线将RESET信号与合适的输入信号进行同步。图67a 所示为在同相输入配置下，如何将 RESET 连接到 VIN+信号进行安全自动复位。图 67b 显示了如何配置 VIN+/ RESET 信号 ，使来自微控制器的 RESET 信号 输入处于写输出-关断写状态。同样，图 67c和图 67d 显示了自动复位和微控制器复位安全配置的反相输入设置。

To resume normal switching operation following a fault condition (FAULT output low), the RESET pin must first be asserted low in order to release the internal fault latch and reset the FAULT output (high). Prior to asserting the RESET pin low, the input (VIN) switching signals must be configured for an output (VOL) low state. This can be handled directly by the microcontroller or by hardwiring to synchronize the RESET signal with the appropriate input signal. Figure 67a shows how to connect the RESET to the VIN+ signal for safe automatic reset in the noninverting input configuration. Figure 67b shows how to configure the VIN+/RESET signals so that a RESET signal from the microcontroller causes the input to be in the “output-off”,state. Similarly, Figures 67c and 67d show automatic RESET and microcontroller RESET safe configurations for the inverting input configuration.

15、用户配置QX316J输出侧RG和可选电阻器User-Configuration of the QX316J Output Side RG and Optional Resistor RC;

栅极电阻RG（以及VCC2和VEE）的大小决定了栅极充/放电电流（ION,PEAK和IOFF,PEAK）的最大值，因此应谨慎选择以匹配 被驱动IGBT的尺寸。通常希望栅极充电电流峰值略小于放电电流峰值 (ION,PEAK<IOFF,PEAK ）。对于这种情况，可以使用一个可选的电阻（RC）和RG来独立测定ION,PEAK和IOFF,PEAK，而不需要使用转向二极管。作为示例，参考图68。假设RG 已经确定，并且设计IOH,PEAK =0.5 A，RC的值可以用下面的方

法估计：The value of the gate resistor RG (along with VCC2 and VEE) determines the maximum amount of gate-charging/dis charging current (ION,PEAK and IOFF,PEAK) and thus should be carefully chosen to match the size of the IGBT being driven. Often it is desirable to have the peak gate charge current be somewhat less than the peak discharge current (ION,PEAK<IOFF,PEAK). For this condition, an optional resistor (RC) can be used along with RG to independently determine ION,PEAK and IOFF,PEAK without using a steering diode. As an example, refer to Fig 68. Assuming that RG is already determined and that the design IOH,PEAK = 0.5A, the value of RC can be estimated in the following way:

$$RC + RG = \frac{[VCC2 - VOH - VEE]}{IOH,PEAK}$$

$$= \frac{[4V - (-5V)]}{0.5A}$$

$$= 18\Omega$$

$$RC = 8\Omega$$

16、采用外部电流缓冲器提高输出电流 Higher Output Current Using an External Current Buffer

为了提高 IGBT栅极驱动电流，可以使用非反相电流缓冲器(如图69所示的npn/pnp缓冲器)。反相型与去饱和故障保护电路不兼容，应避免使用。为了在故障条件下保持IGBT的慢关断特性，需要在输入到VEE的缓冲器中连接一个10nF的 电容，并在输出和公共 npn/ pnp基极之间插入一个10Ω的电阻。MJD44H11/MJD45H11 适用于最大 8A 的电流。D44VH10/ D45VH10 适用于最大 15A 的电流。To increase the IGBT gate drive current, a non-inverting current buffer (such as the npn/pnp buffer shown in Figure 69) may be used. Inverting types are not compatible with the desaturation fault protection circuitry and should be avoided. To preserve the slow IGBT turn-off feature during a fault condition, a 10nF capacitor should be connected from the buffer input to VEE and a 10 Ω resistor inserted between the output and the common npn/ pnp base. The MJD44H11/MJD45H11 pair is appropriate for currents up to 8A maximum. The D44VH10/ D45VH10 pair is appropriate for currents up to 15A maximum.

Figure 67c. safe hardware reset for inverting input configuration

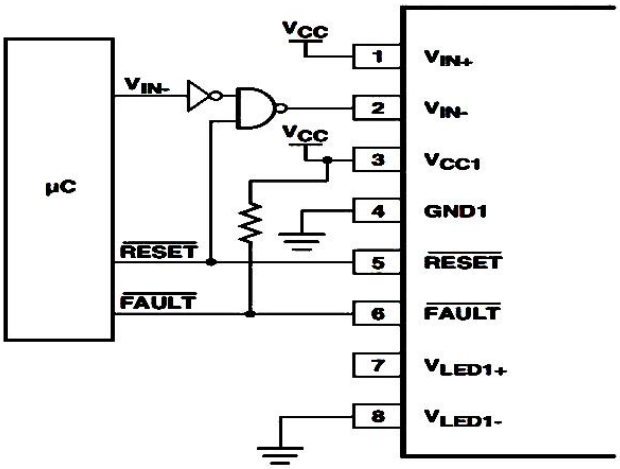


Figure 67d. safe hardware reset for inverting input configuration (automatically resets for every VIN- input)

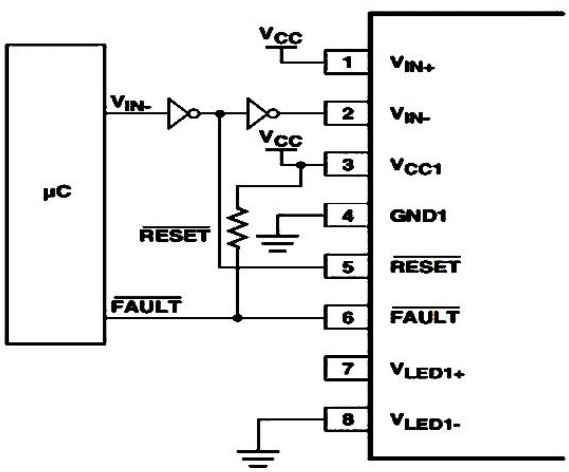


Figure 68. use of Rc to further limit ION,

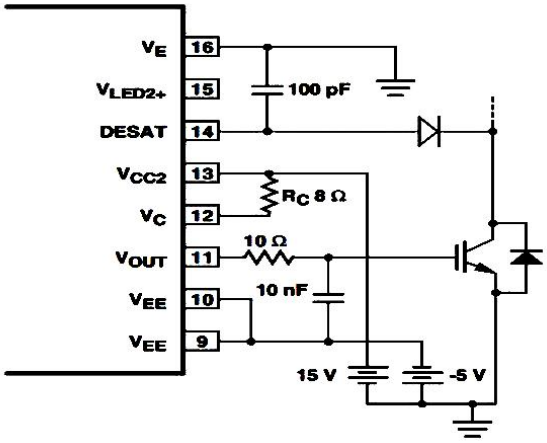
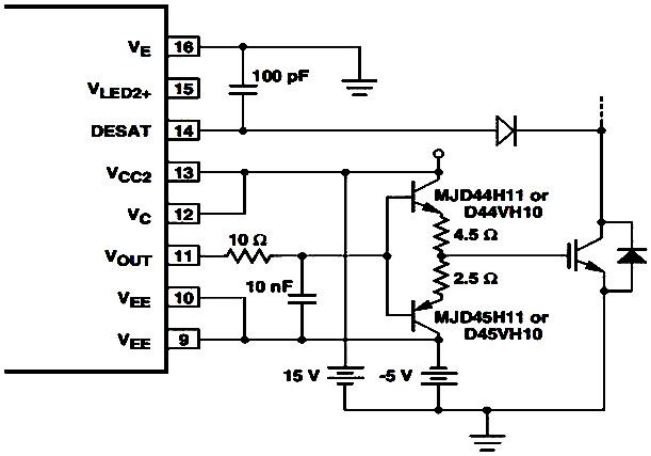


Figure 69. current buffer for increased drive



17、DESAT 二极管和DESAT阈值 DESAT Diode and DESAT Threshold

DESAT二极管的作用是导通正向电流，可以感知IGBT的饱和集电极-发射极电压、VCESAT（当IGBT处于导通状态时）并阻断高压(当IGBT"关断"时)。在IGBT关断的短时间内，IGBT集电极到发射极之间通常存在非常高的dVCE/dt电压上升率。这就产生了ICHARGE（ = CD-DSAT×dVCE / dt)充电电流，该充电电流将对电容器CBLANK进行充电。为了尽量减少这种 充电电流，避免误触发DESAT，最好使用快速响应二极管。在图57所示的推荐应用电路中，引脚14上的电压(DESAT) 为VDESAT = VF + VCE，(其中VF为DDESAT的正向开启电压，VCE为IGBT的集电极-发射极电压)。触发DESAT发出信号FAULT条件的VCE值名义上为7V-VF。如果需要，可以通过使用多个DESAT二极管串联来降低该DESAT阈值电压。若 n 为DESAT二极管个数，则标称阈值变为VCE,FAULT(TH) =7V-n x VF。在使用两个二极管代替一个二极管的情况下，可以选择总所需最大反向耐压额定值的一半的二极管。 The DESAT diode’s function is to conduct forward current, allowing sensing of the IGBT’s saturated collector-to emitter voltage, VCESAT, (when the IGBT is “on”) and to block high voltages (when the IGBT is “off”). During the short period of time when the IGBT is switching, there is commonly a very high dVCE/dt voltage ramp rate across the IGBT’s collector-to-emitter. This results in ICHARGE (= CD-DESAT x dVCE/dt) charging current which will charge the blanking capacitor, CBLANK. In order to minimize this charging current and avoid false DESAT triggering, it is best to use fast response diodes. In the recommended application circuit shown in Fig 57, the voltage on pin 14 (DESAT) is VDESAT = VF + VCE, (where VF is the forward ON voltage of DDESAT and VCE is the IGBT collector-to-emitter voltage). The value of VCE which triggers DESAT to signal a FAULT condition, is nominally 7V– VF. If desired, this DESAT threshold voltage can be decreased by using multiple DESAT diodes in series. If n is the number of DESAT diodes then the nominal threshold value becomes VCE,FAULT(TH) = 7V– n x VF. In the case of using two diodes instead of one, diodes with half of the total required maximum reverse-voltage rating may be chosen.

◆ 电源/布局注意事项 Power/Layout Considerations

1、在最大允许额定功率（RG的调整值）范围内运行Operating Within the Maximum Allowable Power Ratings (Adjusting Value of RG)

在选择RG值时，必须确认QX316J的功耗在最大允许功耗范围内。

When choosing the value of RG, it is important to confirm that the power dissipation of the QX316J is within the maximum allowable power rating.

执行此操作的步骤是:

The steps for doing this are:

（1）计算最小期望RG;

Calculate the minimum desired RG;

（2）参考图73计算该部分的总功耗。(每个周期提供给QX316J的平均开关能量vsRG） Calculate total power dissipation in the part referring to Fig 73. (Average switching energy supplied to QX316J per cycle vs. RG plot)

(3) 将在步骤#2中计算的输入、输出功耗与QX316J的最大推荐功耗进行比较。（如果超过最大推荐水平，可能需要提 高RG值以降低开关功率，并重复步骤2。） Compare the input and output power dissipation calculated in step #2 to the maximum recommended dissipation for the QX316J. (If the maximum recommended level has been exceeded, it may be necessary to raise the value of RG to lower the switching power and repeat step #2.)

例如，在满足一下条件的情况下，可以计算总输入输出功率损耗： As an example, the total input and output power dissipation can be calculated given the following conditions:

.ION, MAX ~ 2.0 A

VCC2 = 18V

VEE =-5V

fCARRIER = 15 kHz

步骤1：根据IOL峰值计算RG最小值： Step 1: Calculate RG minimum from IOL peak specification

为了找到充电峰值IOL，假设栅极初始充电为VEE的稳态值。因此，应用以下关系。

To find the peak charging lOL assume that the gate is initially charged the steady-state value of VEE. Therefore apply the following relationship.

$$RG = \frac{[V_{OH}@650\mu A-(V_{OL}+V_{EE})]}{I_{OL,PEAK}}$$

$$= \frac{[V_{CC2}-1-(V_{OL}+V_{EE})]}{I_{OL,PEAK}}$$

$$= \frac{18V-1V-(1.5V+(-5V))}{2.0A}$$

$$= 10.25\Omega$$

$$= 10.5\Omega \text{ (for a 1\% resistor)}$$

（从图70中可以注意， IOL的实际值可能与从所示的简单模型计算出的值有所不同。NotefromFig70thattherealvalueof IOL may vary from the value calculated from the simple model shown.)

步骤2：计算QX316J中的总功耗： Step2: Calculate total power dissipation in the QX316J

QX316J 总功耗（PT）等于输入端功率（PI）和输出端功率（PO）之和:

The QX316J total power dissipation (PT) is equal to the sum of the input-side power (PI) and output-side power (PO):

PT = PI + PO; PI = ICC1 * VCC1

PO = PO(BIAS) + PO,SWTICH = ICC2 * (VCC2–VEE) + ESWITCH * fSWITCH

PO(BIAS) = QX316J 中由于器件偏置导致的稳态功耗

PO(BIAS) = steady-state power dissipation in the QX316J due to biasing the device.

PO(SWITCH) = QX316J 中由于功率器件栅极充放电而产生的瞬态功率耗散

PO(SWITCH) = transient power dissipation in the QX316J due to charging and discharging power device gate.

ESWITCH =在一个开关周期内，由于功率器件的开关而耗散在QX316J中的平均能量(μJ/cycle)。

ESWITCH = Average Energy dissipated in QX316J due to switching of the power device over one switching cycle (μJ/cycle).

高频开关=平均载波信号频率；fSWITCH = average carrier signal frequency

对于RG=10.5，从图71中读取的值是ESWITCH=6.05μJ。假设最坏情况下平均ICC1 = 16.5mA

（由ICC1H和ICC1L的平均值给出）。类似于平均ICC2 =5.5mA；For RG= 10.5, the value read from Fig 71 is ESWITCH= 6.05 μJ. Assume a worst-case average ICC1 = 16.5mA (which is given by the average of ICC1H and ICC1L). Simiarly the average ICC2 = 5.5mA;

PI = 16.5mA * 5.5 V = 90.8mW ； PO = PO(BIAS) + PO,SWITCH

= 5.5mA * (18 V– (–5 V)) + 6.051 μJ * 15 kHz

= 126.5mW + 90.8mW

= 217.3mW

步骤3： 将计算出的功耗与QX316J的绝对最大值进行比较； Step 3: Compare the calculated power dissipation with the absolute maximum values for the QX316J: For the example

P I = 90.8mW < 150mW (abs. max.) ； PO = 217.3mW < 600mW (abs. max.) OK OK

因此，本例没有超过功耗绝对最大额定值。 Therefore, the power dissipation absolute maximum rating has not been exceeded for the example.

Figure 70. Typical peak ION and IOFF currents vs. Rg (for AT316J output driving an IGBT rated at 600 V/100 A)

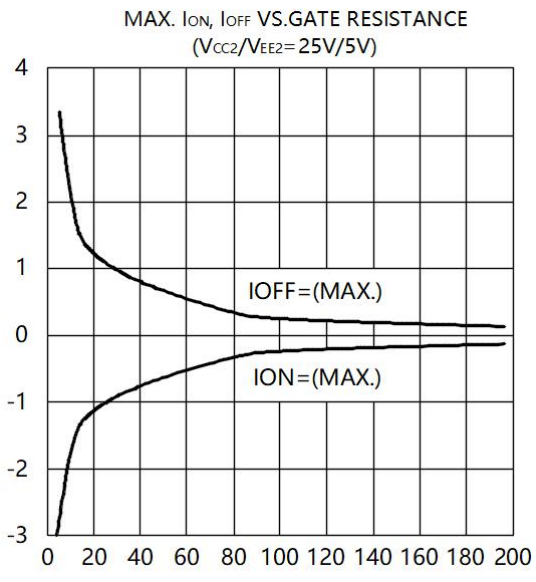
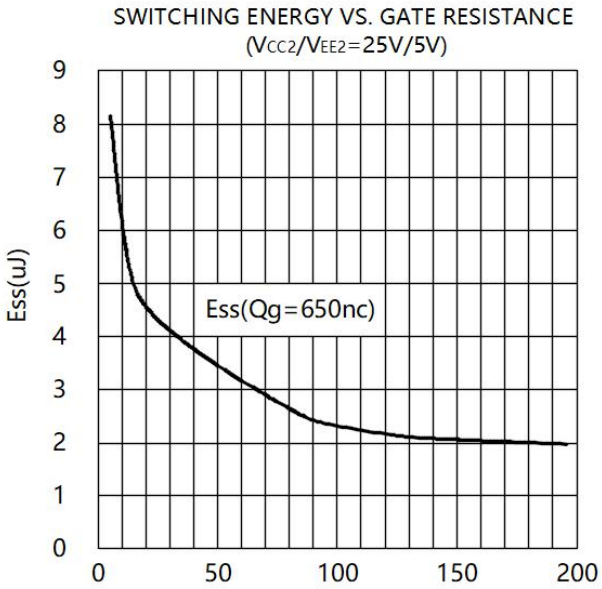


Figure 71. switching energy plot for calculating average pswitch (for AT316J output driving an IGBT rated at 600 V/100 A)



◆ 热模型 Thermal Model

AT316J 设计通过输入 IC 的引脚 4 和输出 IC 的引脚 9 和 10 来散热。(为此，输出侧有两个 VEE 引脚，即引脚 9 和 10) 通过其 他引脚或通过封装直接进入环境的热流被认为可以忽略不计 ，此处不予建模。

The AT316J is designed to dissipate the majority of the heat through pins 4 for the input IC and pins 09 and 10 for the output IC. (There are two VEE pins on the output side, pins 9 and 10, for this purpose.) Heat flow through other pins or through the package directly into ambient are considered negligible and not modeled here.

为了实现绝对最大规格中规定的功耗 ，引脚 4、9 和 10 必须连接地层。只要不超过最大功率规格 ，125气的绝对最大结温规格 是对功耗的唯一其他限制。结温可通过以下公式计算 :In order to achieve the power dissipation specified in the absolute maximum specification, it is imperative that pins 4, 9, and 10 have ground planes connected to them. As long as the maximum power specification is not exceeded, the only other limitation to the amount of power one can dissipate is the absolute maximumjunction temperature specification of 125。C. Thejunction temperatures can be calculated with the following equations:

Tji = pi (qi4 + q4A) + TA

Tjo = po (qo9,10 + q9,10A) + TA

其中Pi =输入IC的功率，Po=输出IC的功率。由于q4A和q9,10A取决于PCB布局和气流，因此可能无法得到它们的准确 数值。因此，可用一下公式更精确地计算结温： Where Pi = power into input IC and Po = power into output IC. Since q4A and q9,10A are dependent on PCB layout and airflow, their exact number may not be available. Therefore, a more accurate method of calculating the junction temperature is with the following equations:

Tji = Piqi4 + TP4

Tjo = Poqo9,10 + TP9,10 Copyright ©2023 Qunxin All Rights Reserve

然而，这些方程要求用QX316J封装边缘引脚上的热电偶测量引脚4和引脚9,10的温度 These equations, however, require that the pin 4 and pins 9, 10 temperatures be measured with a thermal couple on the pin at the QX316J package edge.

从前期的功耗计算实例可知：Pi=90.8mW,Po=314mW,TA=100℃，，假设如下图73所示的热模型 From the earlier power dissipation calculation example: Pi = 90.8mW, Po = 314mW, TA = 100°C, and assuming the thermal model shown in Fig 73 below.

Tji = (90.8mW)(60°C/W + 50°C/W) + 100°C = 110°C

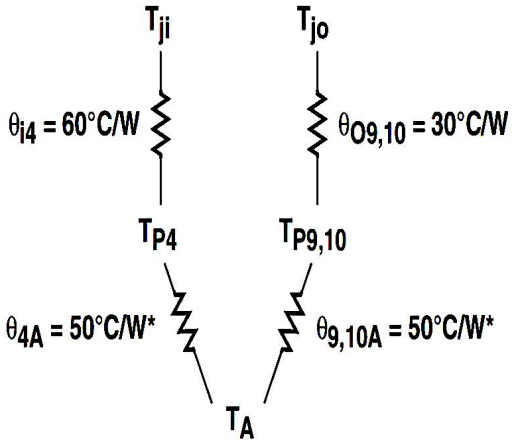
Tjo = (240mW)(30°C/W + 50°C/W) + 100°C = 119°C

两者都在125°C的绝对最大规格范围内。然而，如果我们假设最坏的PCB布局和没有气流的情况下，其中估计的q4A和 q9,10A 为 100°C/W。则结温变为: Both of which are within the absolute maximum specification of 125°C. If we, however, assume a worst case PCB layout and no air flow where the estimated q4A and q9,10A are 100°C/W. Then the junction temperatures become: Tji = (90.8mW)(60°C/W + 100°C/W) + 100°C = 115°C Tji = (240mW)(30°C/W + 100°C/W) + 100°C = 131°C

输出IC结温度超过最大规格125℃. 在这种情况下，需要对PCB的布局和气流进行设计，使输出IC的结温度不超过125℃. The output IC junction temperature exceeds the absolute maximum specification of 125°C. In this case, PCB layout and airflow will need to be designed so that the junction temperature of the

output IC does not exceed 125°C. 如果图72中热模型的计算结温高于125°C，为了更准确地估计结温，需要在最恶劣的工作环境下测量9引脚和10引脚的温度（在包装边缘处) If the calculated junction temperatures for the thermal model in Fig 72 is higher than 125°C, the pin temperature for pins 9 and 10 should be measured (at the package edge) under worst case operating environment for a more accurate estimate of the junction temperatures

Figure 72. AT316Jthermal model



Tji =输入端 IC 结温

Tji =junction temperature of input side IC

Tjo =输出端 IC 结温

Tjo =junction temperature of output side IC

TP4 =封装边缘的引脚 4 温度

TP4 = pin 4 temperature at package edge

TP9，10 =封装边缘引脚引脚 9 和 10 的温度

TP9，10 = pin 9 and 10 temperature at package edge

θI4 =输入端 IC 到引脚 4 的热阻

θI4 = input side IC to pin 4 thermal resistance

θI9，10 =输出端 IC 到引脚 9 和 10 的热阻

θI9，10 = output side IC to pin 9 and 10 thermal resistance

θ4A = 引脚 4 环境热阻

θ4A = pin 4 to ambient thermal resistance

θ9，10A =引脚 9 和 10 环境热阻

θ9，10A = pin 9 and 10 to ambient thermal resistance

*此处显示的θ5A 和θ9，12A 值是针对图 74 气流合理的 PCB 布局。根据 PCB 布局/气流情况 ,该值可能增加或减少 2 倍 *The θ4A and θ9,10A Values shown here are for PCB layouts shown in Figure 74 with reasonable air flow. This Value may increase or decrease by a factor of 2 depending on PCB layout and air flow.

◆ 印刷电路板布局的注意事项 Printed Circuit Board Layout Considerations

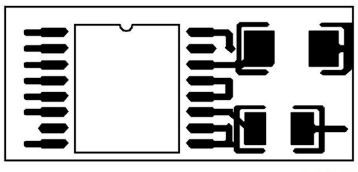
高压隔离电路与任何输入参考电路之间应始终保持足够的间距。必须注意在印刷电路板的两个相邻的高边隔离区之间提 供相同的最小间距。间距不足会降低有效隔离度，增加寄生耦合，降低CMR性能。 Adequate spacing should always be maintained between the high voltage isolated circuitry and any input referenced circuitry. Care must be taken to provide the same minimum spacing between two adjacent high-side isolated regions of the printed circuit board. Insufficient spacing will reduce the effective isolation and increase parasitic coupling that will degrade CMR performance.

电源旁路电容的布线需要特别注意。在开关瞬态过程中，大部分的栅极电荷由旁路电容提供。保持较短的旁路电容跟踪 长度将保证较低的电源纹波和干净的开关波形。 The placement and routing of supply bypass capacitors requires special attention. During switching transients, the majority of the gate charge is supplied by the bypass capacitors. Maintaining short bypass capacitor trace lengths will ensure low supply ripple and clean switching waveforms.

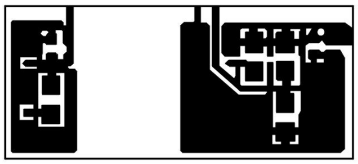
接地平面连接对于引脚4(GND1)和引脚9和10(VEE)是必要的，以实现最大的功耗，因为QX316J的设计是为了消耗通 过这些引脚产生的大部分热量。实际功耗将取决于应用环境(PCB布局、气流、部件放置等)，有关如何估计结温的详细信 息，请参阅热模型部分。 引脚4(GND1)和引脚9和10(VEE)需要接地，以实现最大功耗，因为QX316J设计用于耗散通过这些引脚产生的大部分 热量。实际功耗将取决于应用环境(PCB布局、气流、部件放置等。)关于如何估计结温的详细信息，请参阅热模型部分。 Ground Plane connections are necessary for pin 4 (GND1) and pins 9 and 10 (VEE) in order to achieve maximum power dissipation as the QX316J is designed to dissipate the majority of heat generated through these pins. Actual power dissipation will depend on the application environment (PCB layout, air flow, part placement, etc.) See the Thermal Model section for details on how to estimate junction temperature.。

下面的布局实例具有良好的电源旁路和热特性，PCB占地面积小，信号和供电线路容易连接。这四个例子涵盖了单面和 双面元件布局，以及最小和改进的性能电路。 The layout examples below have good supply bypassing and thermal properties, exhibit small PCB footprints, and have easily connected signal and supply lines. The four examples cover single sided and double sided component placement, as well as minimal and improved performance circuits.

Minimum Components placed on two sides

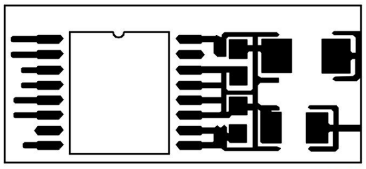


TOP



Total Area=0.39 sq.in Bottom

Maximum Components placed on two sides



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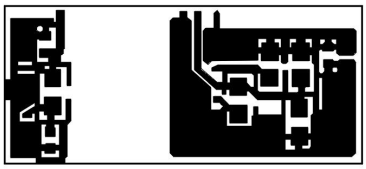
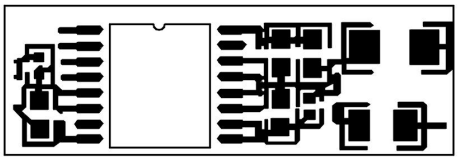


Total Area=0.46 sq.in Bottom

Minimum Components placed on one sides



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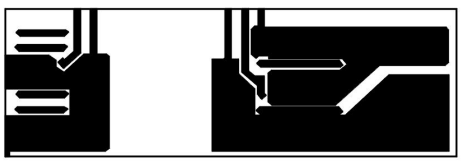
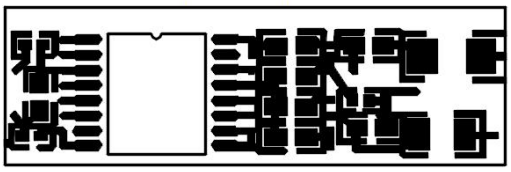
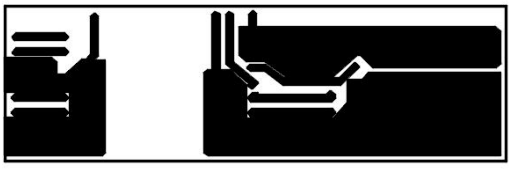


Total Area=0.54 sq.in Bottom

Maximum Components placed on one sides



TOP



Total Area=0.61sq.in Bottom

◆ 系统注意事项 System Considerations

传播延迟差Propagation Delay Difference (PDD) QX316J 包括一个传播延迟差异(PDD)规范，旨在帮助设计人员在功率逆变器设计中尽量减少"死区时间"。死区时间是高、 低侧功率晶体管(图57中的Q1和Q2)均关断的时间段。Q1和Q2导通的任何重叠都将导致大电流流过高低压电机导轨之 间的功率器件，这是一个必须防止的潜在灾难性条件。 The QX316J includes a Propagation Delay Difference (PDD) specification intended to help designers minimize “dead time” in their power inverter designs. Dead time is the time period during which both the high and low side power transistors (Q1 and Q2 in Fig 57) are off. Any overlap in Q1 and Q2 conduction will result in large currents flowing through the power devices between the high and low voltage motor rails, a potentially catastrophic condition that must be prevented.

在给定的设计中，为了最小化死区时间，QX316J驱动Q2的导通应该延迟(相对于QX316J驱动Q1的关断)，这样在最坏 的情况下，当晶体管Q2导通时，晶体管Q1刚好关断，如图74所示。在-40°C到110°C的工作温度范围内，实现该条 件所需的延迟量等于传播延迟差PDDMAX的最大值，即指定为400ns。 To minimize dead time in a given design, the turn-on of the QX316J driving Q2 should be delayed (relative to the turn-off of the QX316J driving Q1) so that under worst-case conditions, transistor Q1 has just turned off when transistor Q2 turns on, as shown in Fig 74. The amount of delay necessary to achieve this condition is equal to the maximum value of the propagation delay difference specification, PDDMAX, which is specified to be 400 ns over the operating temperature range of-40°C to 110°C.

通过最大传播时延差对QX316J开通信号进行延迟保证了最小死区时间为零，但并没有告诉设计者最大死区时间是多少。 最大死区时间相当于最大和最小传播时延差规范的差值，如图75所示。在-40°C到110°C的工作温度范围内，QX316J的 最大死时间为800ns((=400ns-(- 400ns)))。 Delaying the QX316J turn-on signals by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time is equivalent to the difference between the maximum and minimum propagation delay difference specifications as shown in Fig 75. The maximum dead time for the QX316J is 800 ns (= 400ns- (-400ns)) over an operating temperature range of-40°C to 110°C.

值得注意的是，用于计算PDD和死区时间的传播延迟是在相同的温度和测试条件下计算的，因为所考虑的光耦通常安装 在彼此接近的位置，并且是开关相同的IGBTs。 Note that the propagation delays used to calculate PDD and dead time are taken at equal temperatures and test conditions since the optocouplers under consideration are typically mounted in close proximity to each other and are switching identical IGBTs

Figure 74. Minimum LED Skew for zero Dead Time

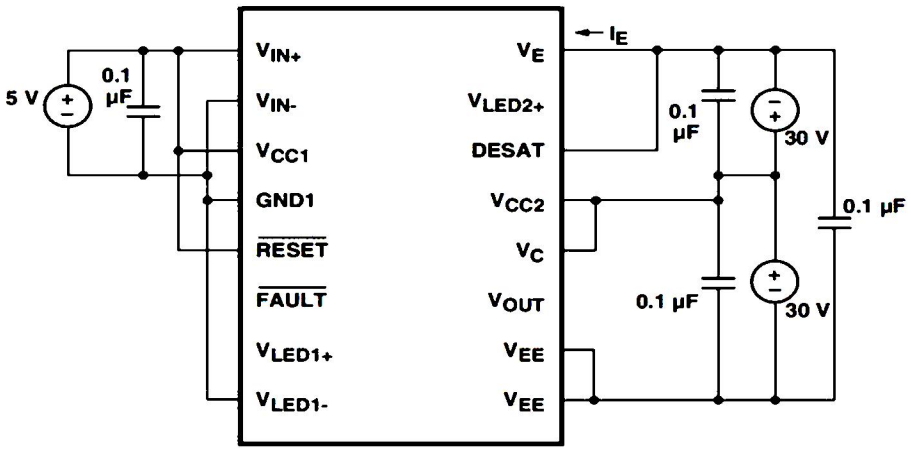
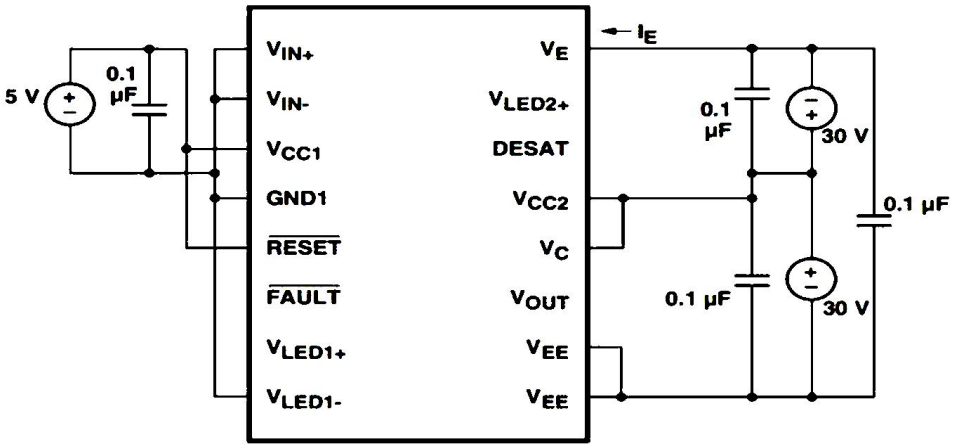
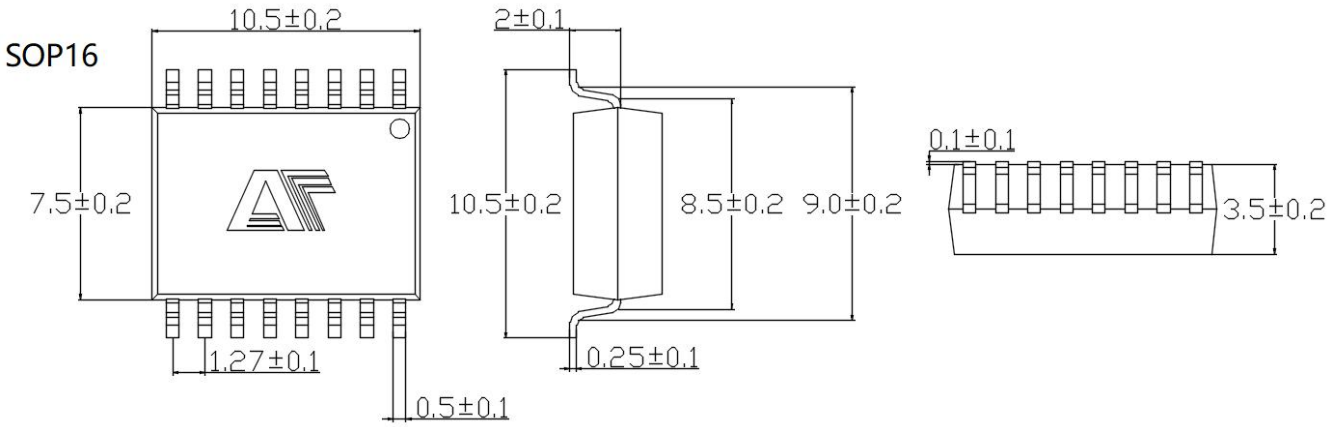


Figure 75. waveforms for Dead Time calculation

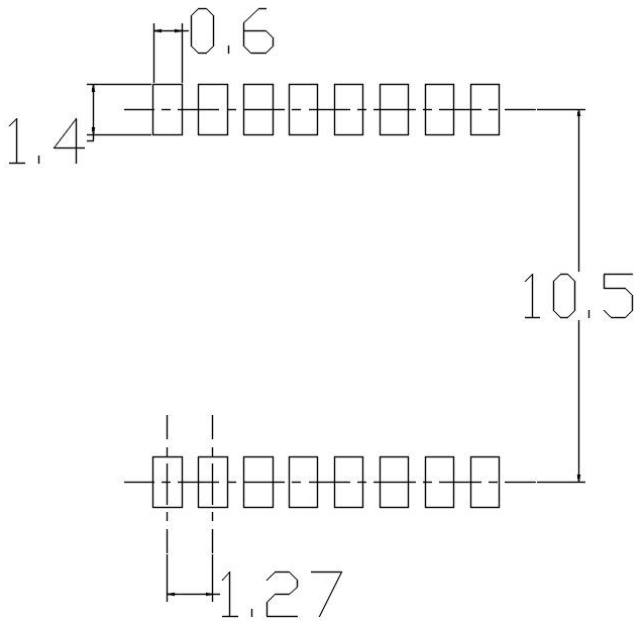


◆ 外形尺寸Overall dimension



推荐焊盘：

Recommended



单位：mm

◆ 产品型号命名规则 Order code

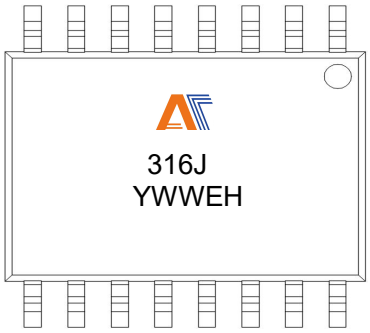
AT 316J - UN Y - W (V) (ZZ)

① ② ③ ④ ⑤ ⑥ ⑦

① 公司代码 Company Code (AT: 奥特 Aote)
② 产品系列 Product Series (316J)
③ 框架类型 Lead Frame (Cu: 铜框架 Copper,Fe: 铁框架 Ferrum)
④ 树脂类型 Epoxy Type (H: 无卤 Halogen-free)
⑤ 封装形式 Package (D:DIP, S:SMD)
⑥ 器件工作温度范围 Device Operating Temperature Range (特殊范围需填或者空白 Special Range need to be filled in or left blank)
⑦ 内部补充代码 Internal Supplementary Code (数字或者空白 Number or None)

◆ 印字信息 Marking Information

- 印字中“ ”为奥特品牌LOGO
  “ ”denotes LOGO
- 印字中“Y”代表年份; A(2018),B(2019),C(2020) ... ...
  “Y”denotes YEAR: A(2018), B(2019), C(2020) ... ...
- 印字中“WW”代表周号
  “WW”denotes Week’s number
- 印字中“ E”代表内部代码
  “E”denotes Internal code
- 印字中的“H”代表无卤
  “H”denotes Halogen-free

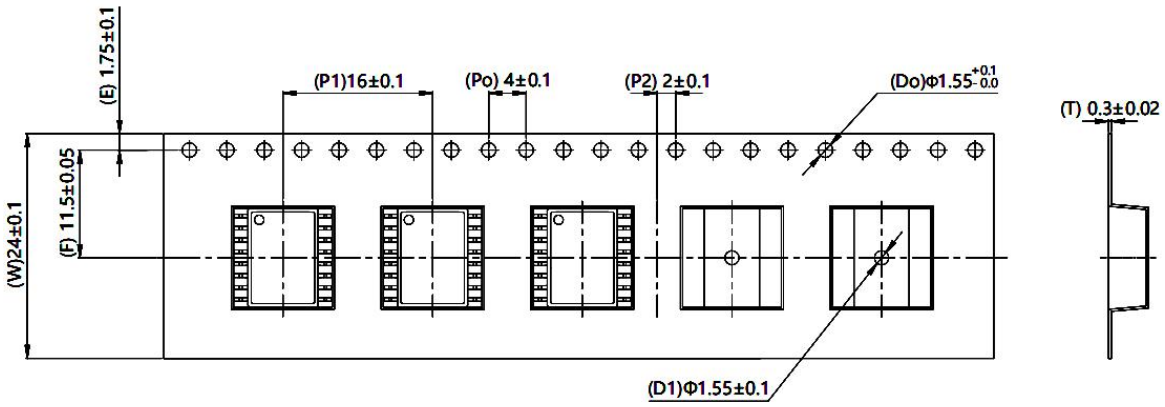


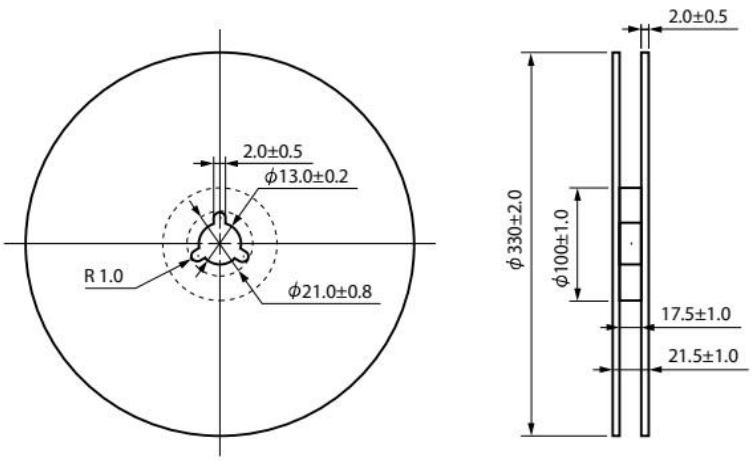
◆ 包装packing

封装形式	包装方式	盘数量	盒数量	箱数量	静电袋规格	盒规格	箱(双瓦楞)规 格	备注
SOP16	Reel (ϕ330mm 蓝盘)	850 只/盘	2 盘/盒	8 盒/箱	450*390*0.1mm	340*340*75 mm	650*375*365mm	首端空 50 个空格, 末端空 100 个空格
Package Type	Packing Form	Quantity per Reel	Quantity per Box	Quantity per Carton	Antistatic Bag Specification	Box Specification	Carton Specification	Note
SOP16	Reel (ϕ330mm Blue)	850 pcs/reel	2 reels/box	8 boxes/ctn	450*390*0.1mm	340*340*75 mm	650*375*365mm	Leave 50 Spaces at the beginning and 100 Spaces at the end

• 编带包装 Tape & Reel

1) 每卷数量：850 只；Qty/reel：850 pcs；
2) 每箱数量：13600 只；Qty/ctn：13600 pcs；
3) 内包装：每盒 2 盘；Inner packing：2 reels/box；
4) 示意图 Schematic:



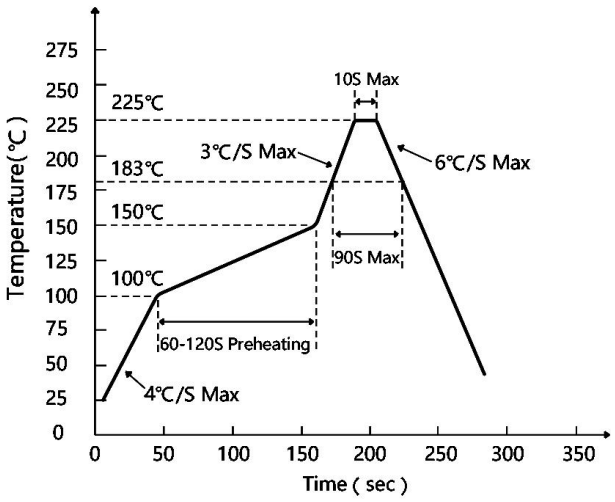


单位：mm

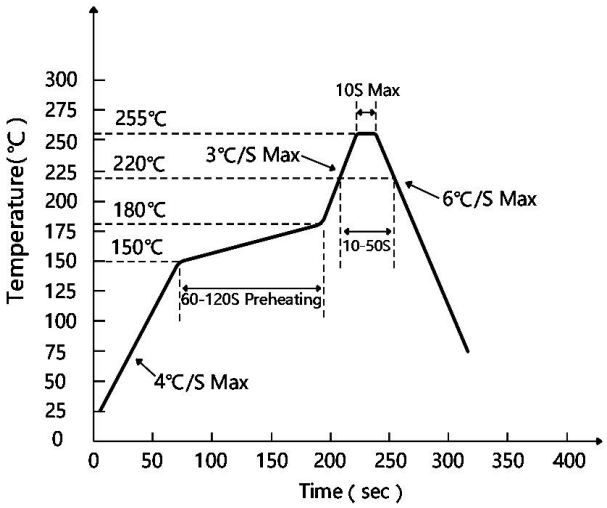
◆ 可靠性测试 Reliability Test Items And Conditions

实验项目 Test Items	参考标准 Reference	实验条件 Test Conditions	时间 Time	样品数 Quantity	判据 Criterion
可焊性 Solderability	JESD22-B102	Tsol=（245±5）℃, t=5s;	1 次1 times	22	0/22
耐焊接热 Resistance to Soldering Heat	JESD22-A106	Tsol=（260±5）℃, t=10s	3 次3 times	22	0/22
静电放电 ESD-HBM	JESD22-A114	Ta=25℃, HBM (2000V)	正反各 3 次 P&N 3 times	10	0/10
高温贮存 High emperature Storage	JESD22-A103	Ta=125℃	1000h	22	0/22
低温贮存 Low Temperature Storage	JESD22-A119	Ta= -55℃	1000h	22	0/22
冷热冲击 Thermal Shock	JESD22-A104	-55℃(15min)←→ 125℃(15min)	循环 300 次 300 cycles	22	0/22
常温寿命试验 Lifespan Test	JESD22-A108	Ta=25℃, IF=50mA ， Vcc=5V	1000h	22	0/22
高温寿命试验 DC Operating Life	JESD22-A108	Ta=110℃, IF=20mA ， Vcc=5V	1000h	76	0/76
高温高湿偏压 High Temperature High Humidity bias Voltage	JESD22-A101	Ta =85℃ , RH=85% IF=0mA ， VCE=64V	1000h	22	0/22
高温偏压 High Temperature bias Voltage	JESD22-A108	Ta =110℃ , IF=0mA ， VCE=80V	1000h	22	0/22
高压蒸汽试验 High pressure steam test	JESD22-A102	P=15PSIG ， 121℃, 100%RH	96h	22	0/22

◆ 回流焊温度曲线图 Solder Reflow Profile

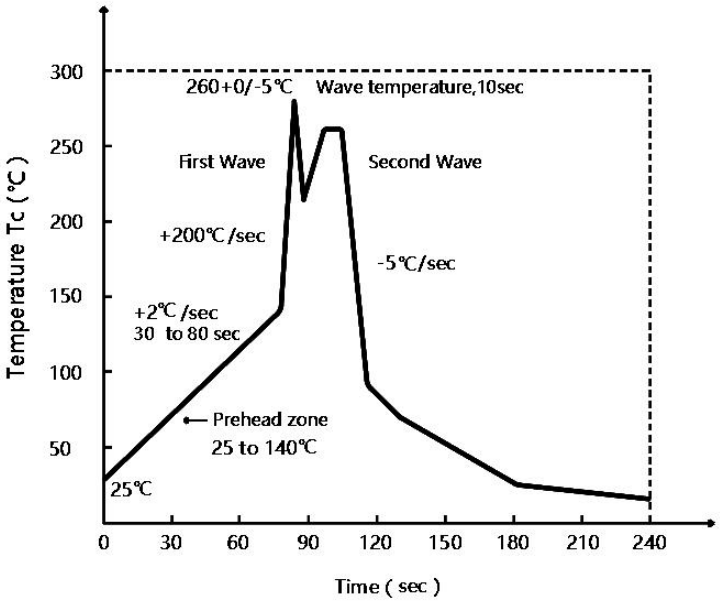


有铅制程 Lead Process



无铅制程 Lead Process

◆ 波峰焊温度曲线图 Wave Soldering Profile



◆ 手工烙铁焊接 Soldering with hand soldering iron

A. 手工烙铁焊仅用于产品返修或样品测试;

Hand soldering iron is only used for product rework or sample testing;

B. 手工烙铁焊要求: 温度 350℃ ± 5℃, 时间≤3s。

Hand soldering iron requirements: Temperature: 350℃ ± 5℃, within 3s.

◆ 注意 Attention

- 奥特半导体实施动态技术迭代机制，产品规格可能随工艺升级调整，最新技术参数以官网发布版本为准。

AOTE implements dynamic technical updates. Specifications are subject to change. Refer to the official website for the latest version.

- 用户需严格遵循本规格书限定的操作条件，因超范围使用（包括但不限于过载、高温、非兼容电路设计）导致的器件失效，不在质量保证范围内。

Users must strictly adhere to specified conditions. Failures caused by misuse (overload, high temperature, incompatible circuits) are excluded from warranty.

- 医疗设备、工业控制等关键场景应用前，需联系技术支持获取定制化验证方案。

Contact technical support for customized validation in critical applications (medical devices, industrial control).

- 本文档有效期至2025年12月31日，后续更新将通过官网公告推送。

This document is valid until Dec 31, 2025. Updates will be notified on the official website.

- 如需对技术参数或应用方案进行进一步确认，欢迎通过以下渠道获取官方支持：

For further clarification on technical specifications or application solutions, please contact us through official channels: